

Block Diagram

PCB STACK UP

6L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

Intel Processor
Sandy Bridge

ULV 17Watt
31*24mm

BGA 1023P

PAGE 3-6

DDR3 1333MT/s (Single Channel B)

DDR3 SO-DIMM-1
STD

4GB Max. Page 16

DDR3 on board

Page 13-14

Channel A

DMI*4

FDI

32.768KHz
BCLK133M
DMI100M
DP120M

USB 2.0

Cougar Point
Platform Controller Hub

- FCBGA package
- Package size: 25 mm x 25 mm
- Ball Count: 989
- Ball pitch: 0.6 mm

PAGE 7-12

LVDS

CRT

HDMI

SATA

LPC

SPI

HDA

PCI-Express

3,5,9

0

2

1

8

USB2.0
Port x3

Page 22

Card Reader

Page 22

BT / WLAN

Page 23

WWAN

Page 24

Webcam

Page 18

Card Reader
Socket

Page 17

SIM Card Socket

Page 24

X1

X1

LAN
RTL8111E

Page 21

WLAN

Page 21

25MHz

RJ 45

Page 21

SYSTEM POWER
+3VS5/+5VS5(RT8223)

PAGE 29

11.6" LED Panel

Page 18

CRT Connector

Page 17

HDMI Connector

Page 19

CPU CORE (RT8165BGQW)

PAGE 30

SYSTEM CHARGER (OZ8681)

PAGE 34

1.05V(RT8240BZ)
1.8V(G5173)

PAGE 33

Dis-charge (SLG55448VTR)
+3VSUS/+3V/+5V/+1.5V/+3VLAVCC

PAGE 35

VCCSA (RT8241EZ)

PAGE 31

2.5"HDD/SSD

Page 25

Accelerometer

Page 25

Touch Pad

Page 27

Keyboard

Page 27

ENC KBC

ENE3930 A2

Page 28

BIOS
SPI Flash

Page 28

AUDIO CODEC

92HD87BX

Page 20

Int SPK

Page 20

Digital MIC

Page 20

MIC JACK

Page 20

Amplifier
Beats

Page 20

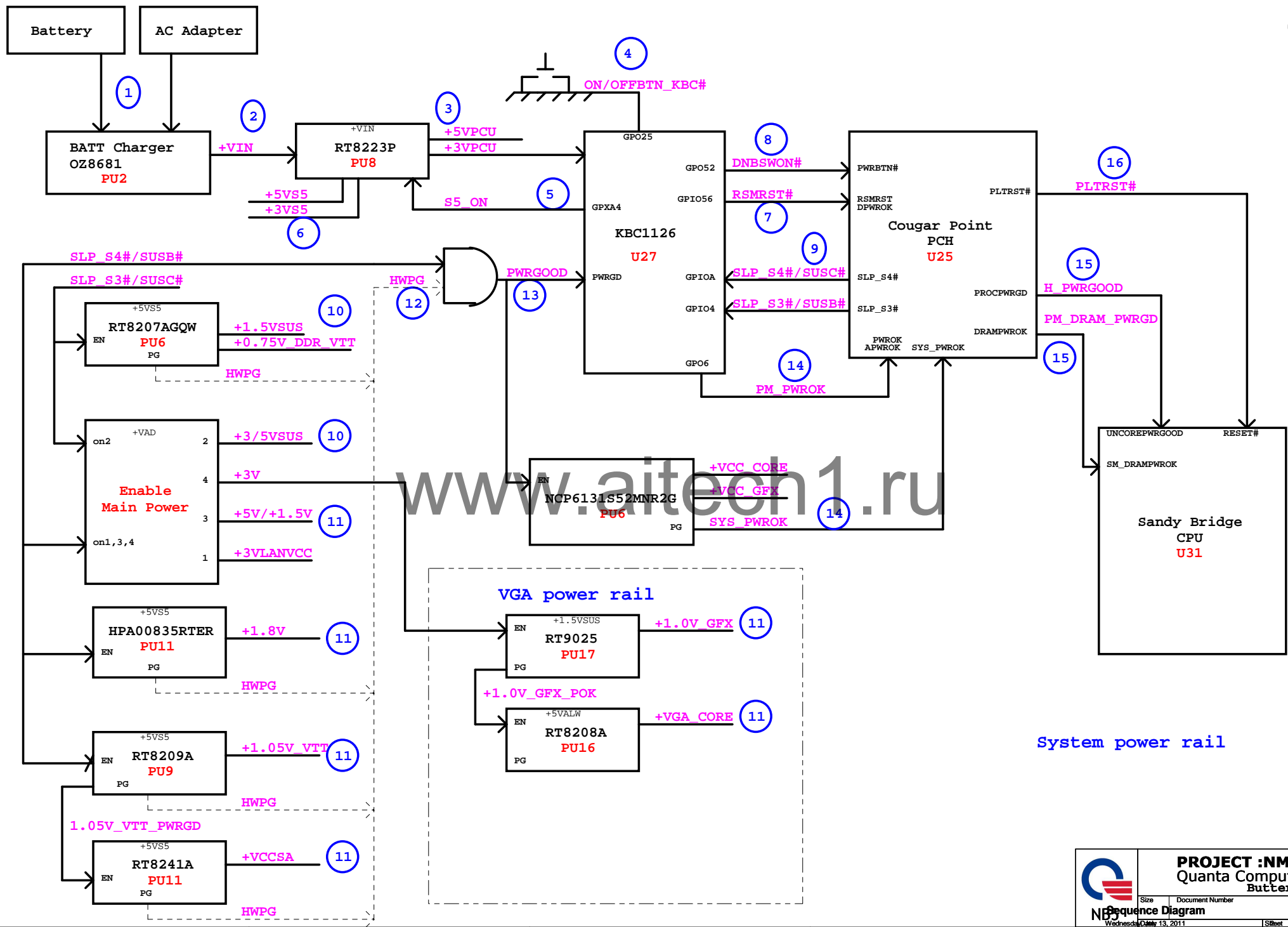
HP JACK

Page 20

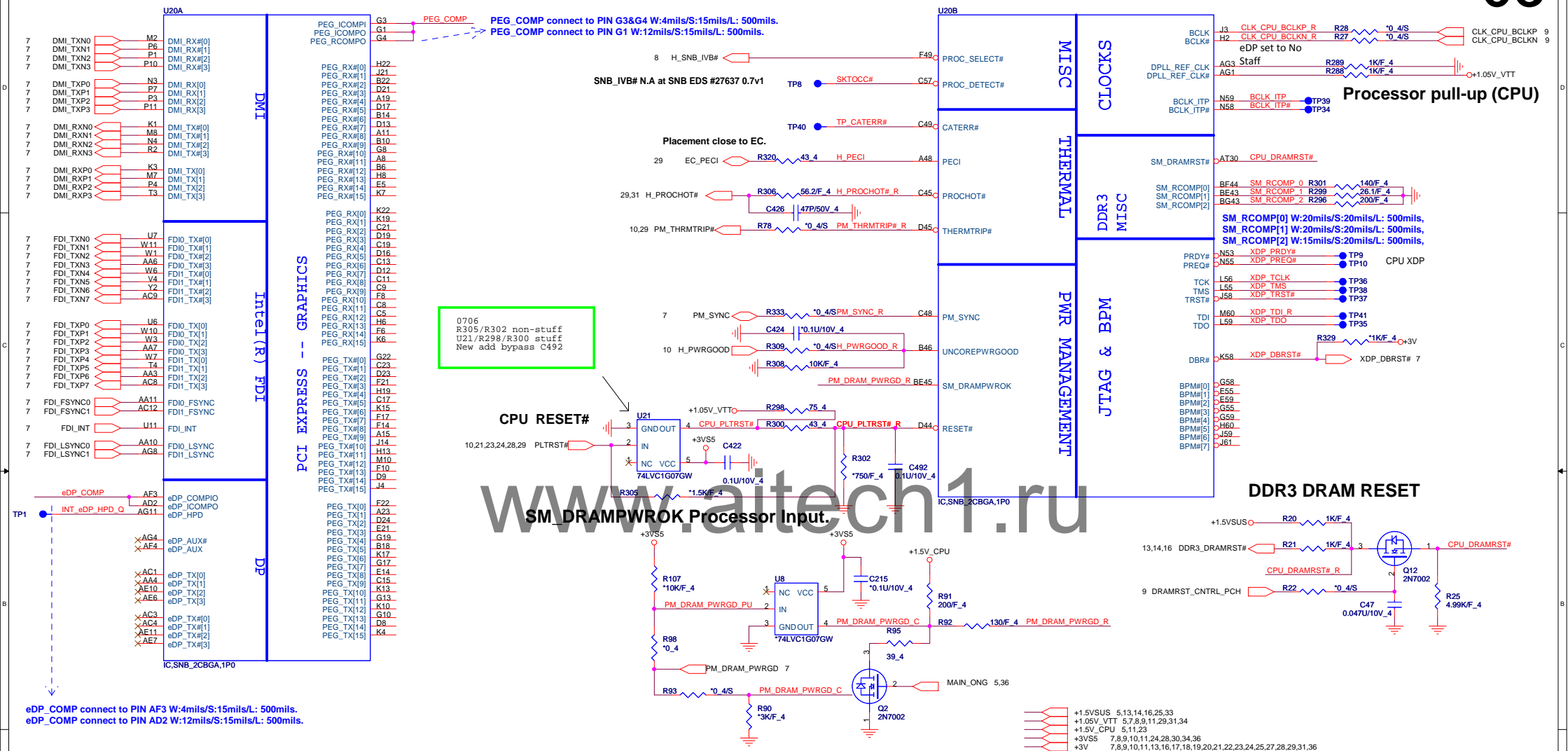


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Sandy Bridge Processor (DMI,PEG,FDI)



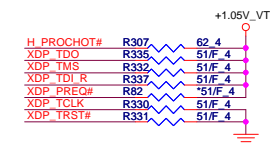
DP & PEG Compensation

+1.05V_VTTO  24.9/F 4 eDP_COMP

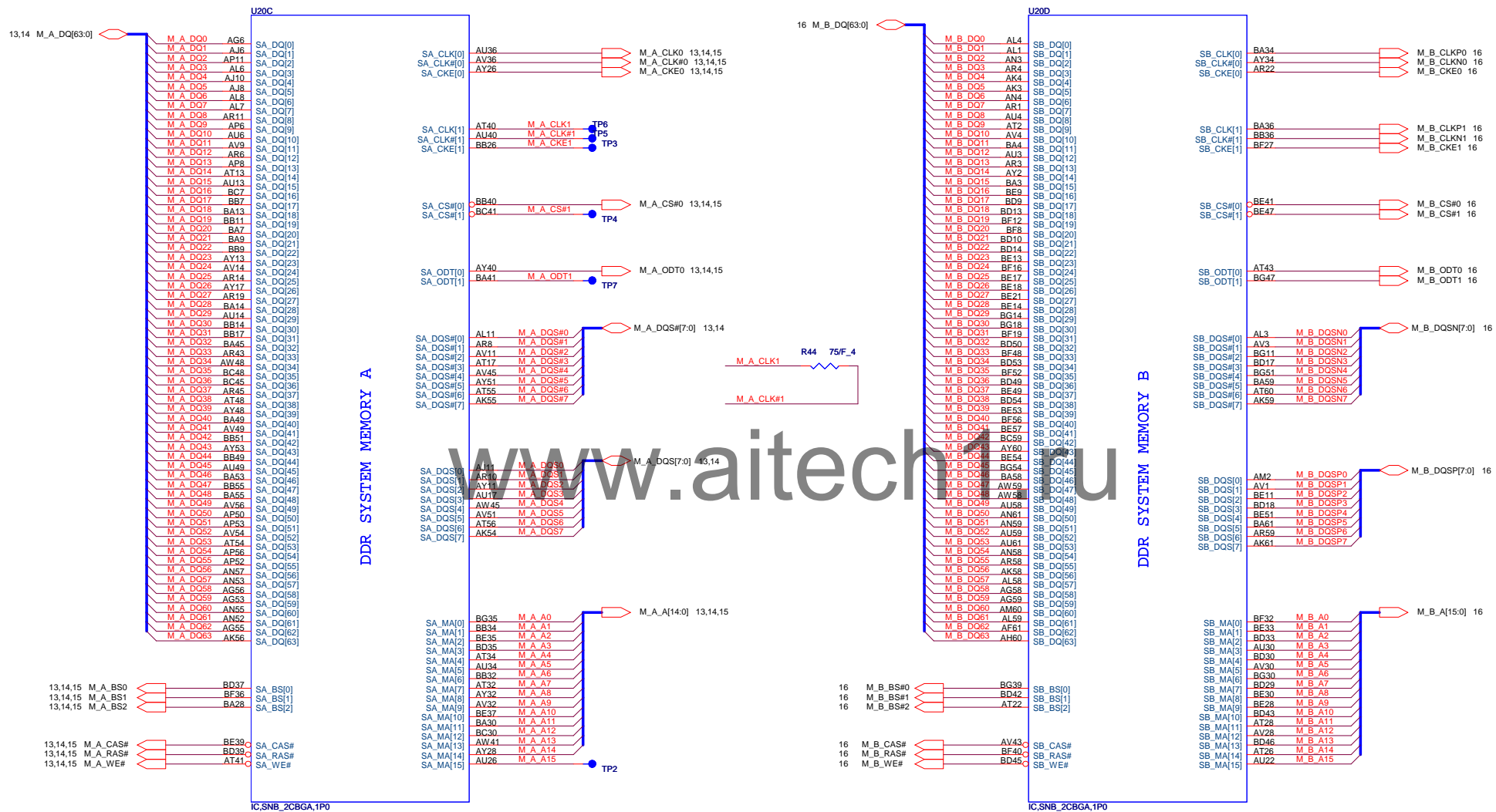
eDP_COMP and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

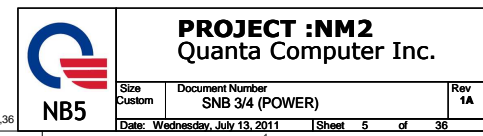
PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms
PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

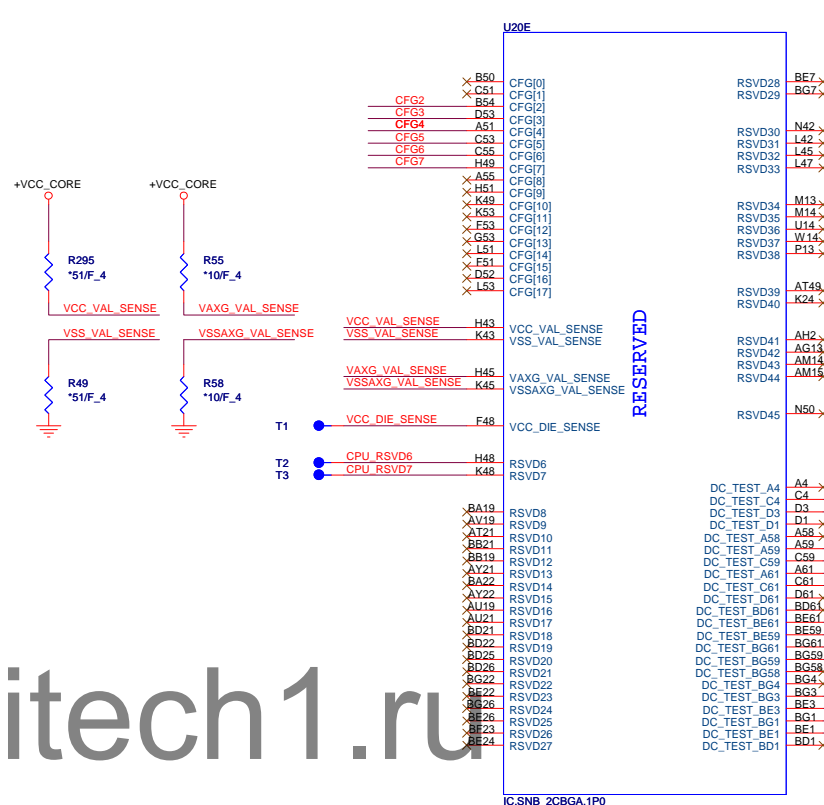
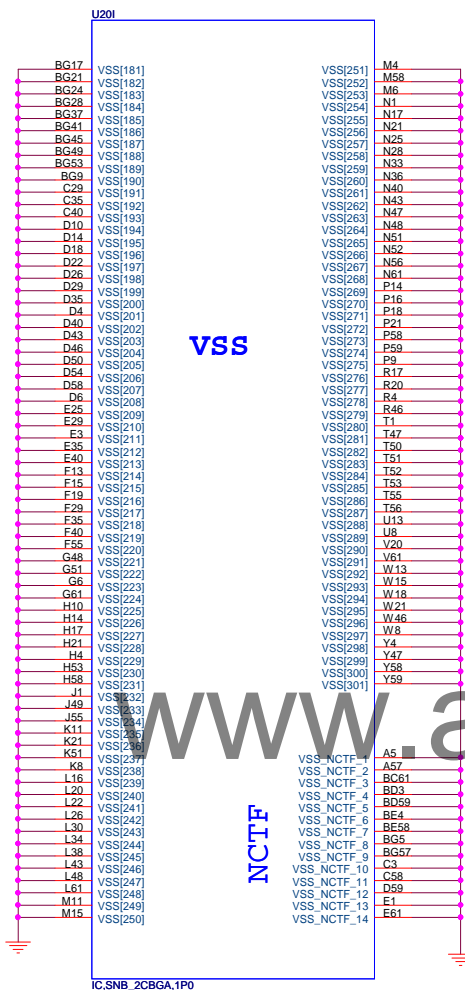
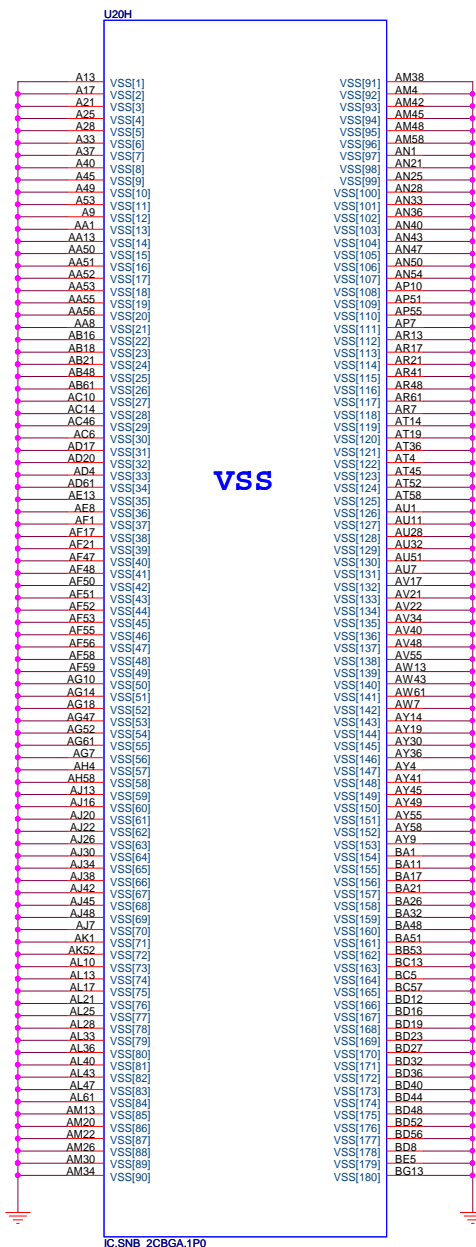
Processor pull-up (CPU)



Sandy Bridge Processor (DDR3)







Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

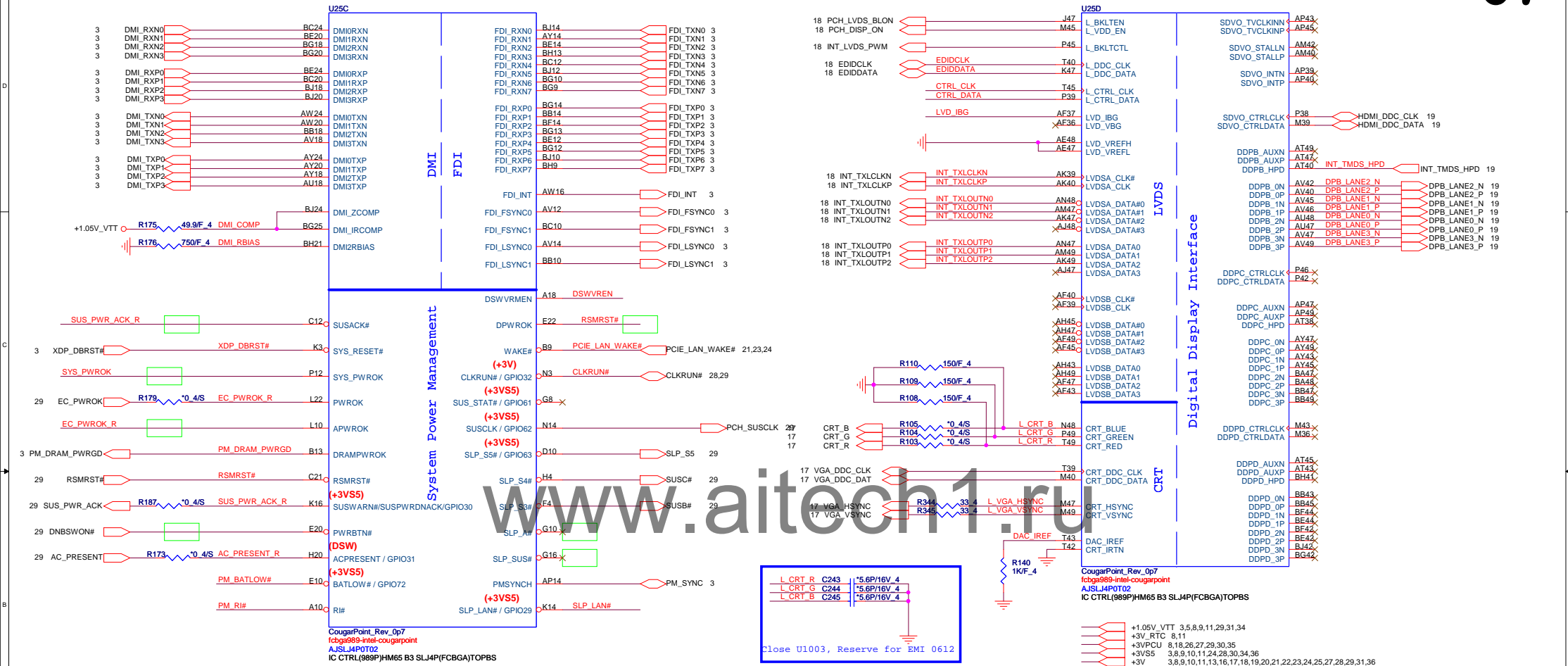


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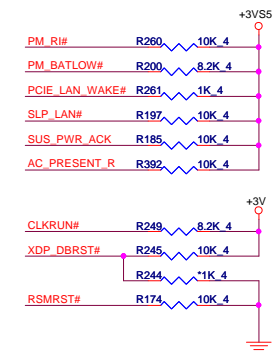
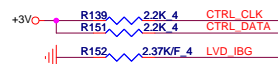
Size Custom	Document Number SNB 4/4 (GND)	Rev 1A
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Cougar Point (DMI,FDI,PM)

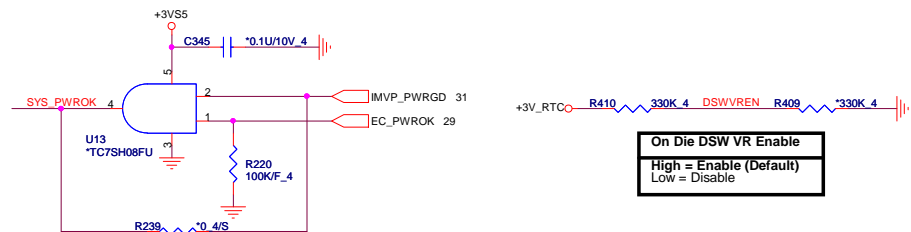
Cougar Point (LVDS,DDI)



PCH Pull-high/low(CLG)

INT LVDS & CRT disable
(DIS only remove)

System PWR_OK(CLG)



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Size Custom Document Number PCH 1/6 (DMI/FDI/VIDEO) Rev 1A
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Cougar Point (HDA,JTAG,SATA)

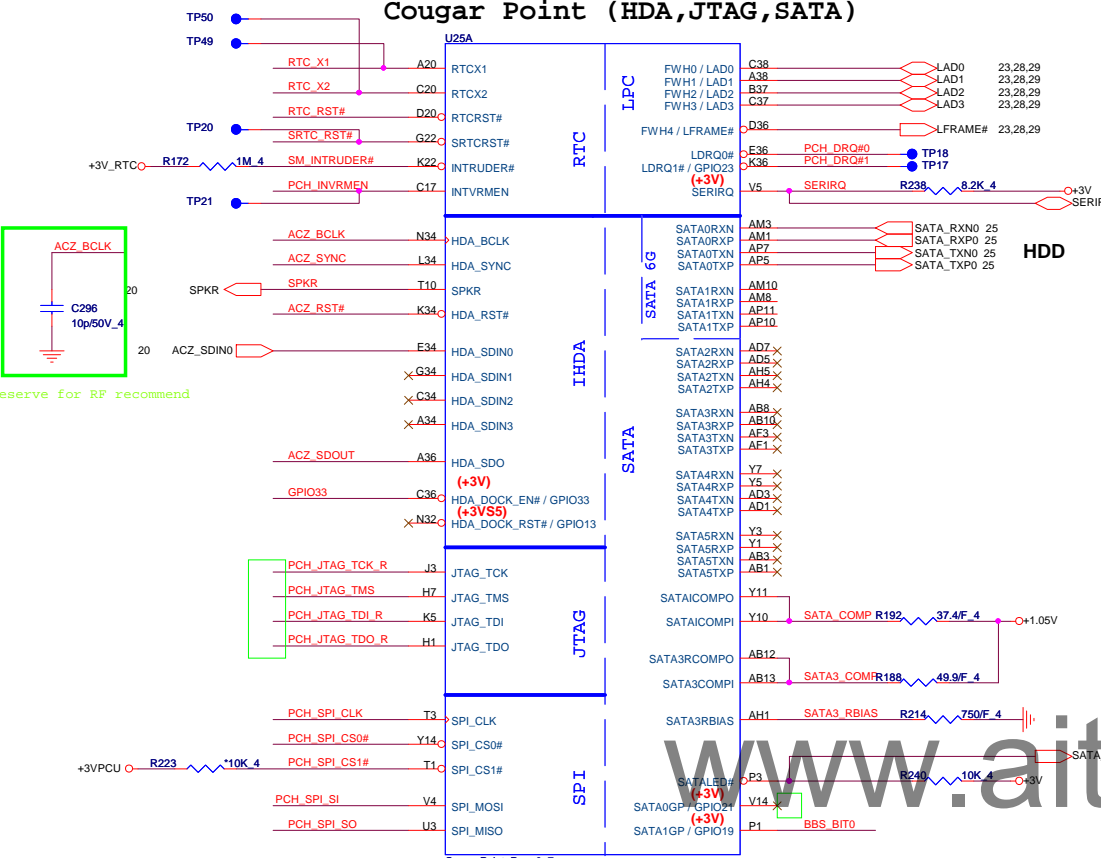


Table with 2 columns: Voltage, Pin/Label. Rows include +1.05V_VTT, +1.8V, +3V_RTC, +3VPCU, +3V, and +3VS5 with their respective pin connections.

RTC Clock 32.768KHz

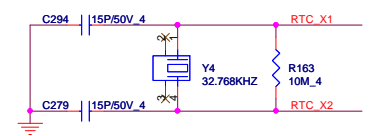
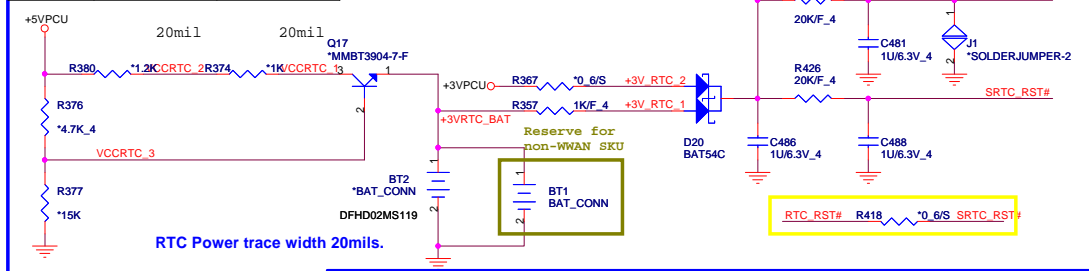
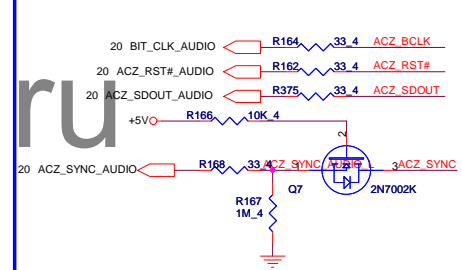


Table with 3 columns: Note, stuff, no stuff. Rows include Non-WWAN SKU, BT1, and WWAN SKU with their respective part numbers.

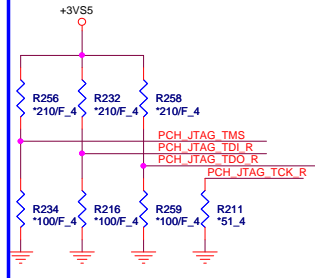
RTC Circuitry(RTC)



HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)

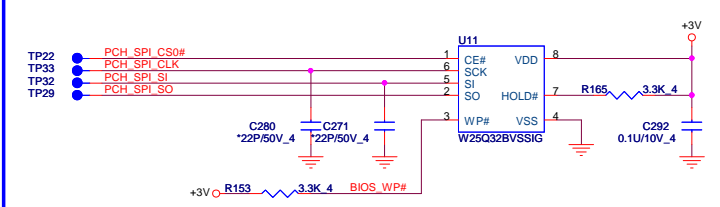


Table with 3 columns: Vender, Size, P/N. Rows include EON, Winbond, and Socket with their respective specifications.

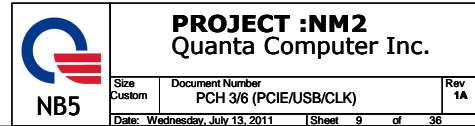
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR <div>Different from Calpella</div>	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td>0</td><td>1</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	1	LPC	<div>(Need external pull-down for LPC BIOS)</div> <div>Default weak pull-up on GNT0/1#</div>
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	1	LPC											
GPIO19 <div>Different from Calpella</div>	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 <div>Different from Calpella</div>	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

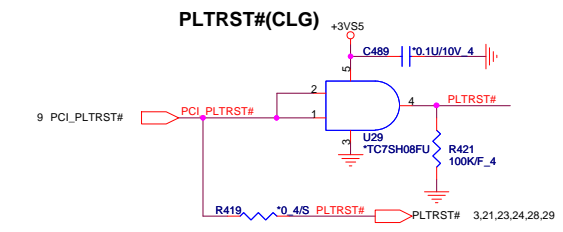
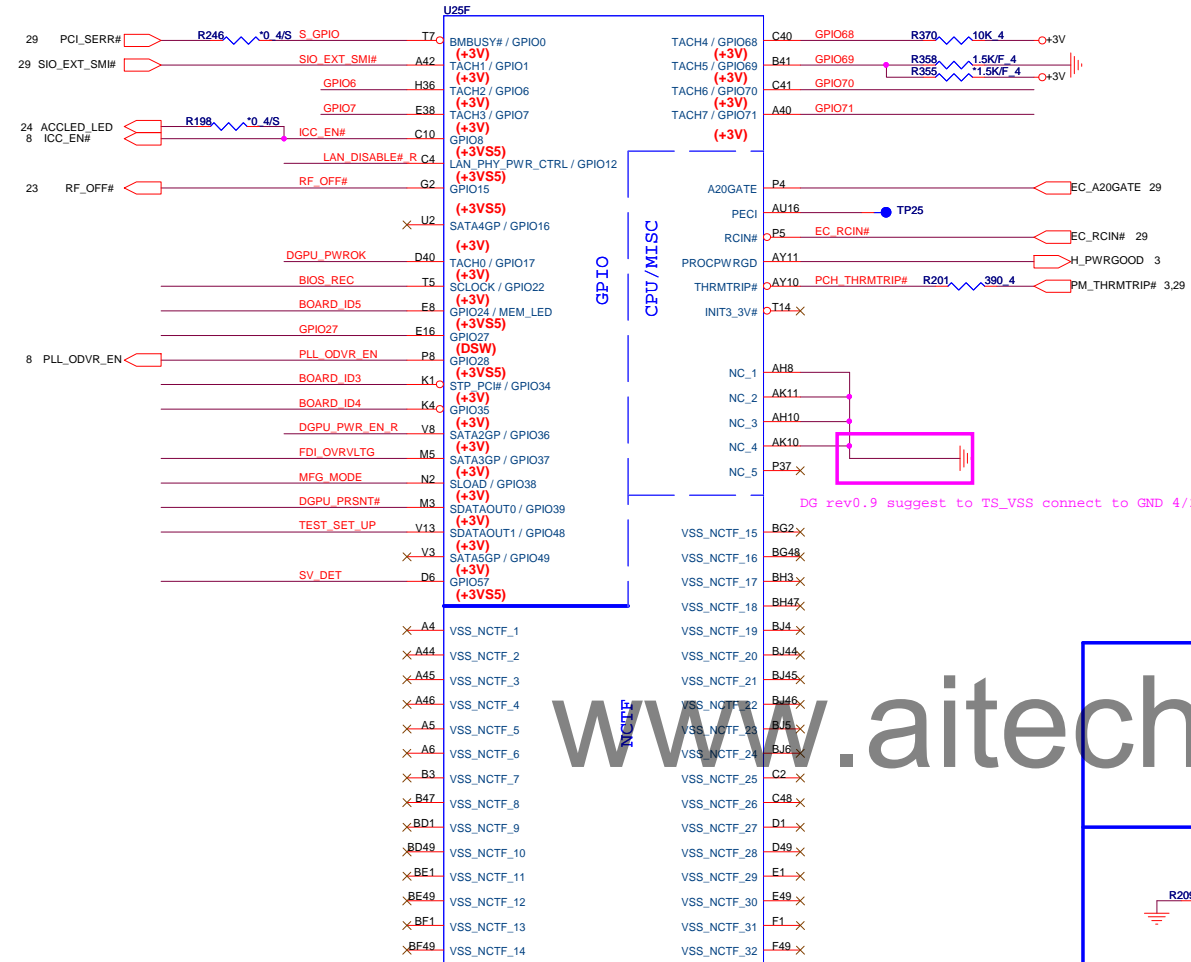
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NB5

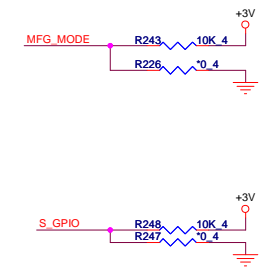
Size Custom Document Number PCH 2/6 (SATA/HDA/SPI) Rev 1A
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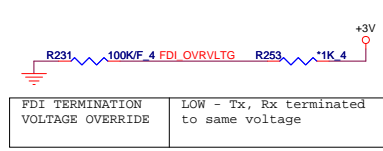
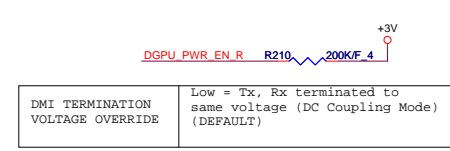
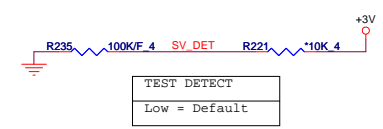
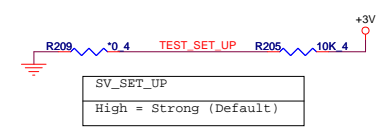
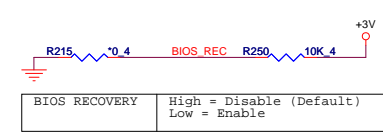
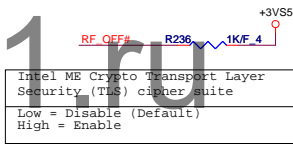
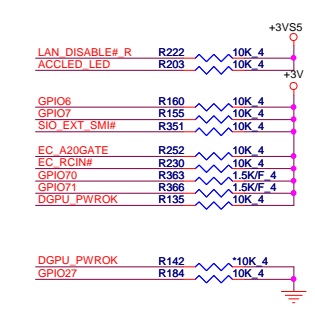
Cougar Point (GPIO,VSS_NCTF,RSVD)



MFG-TEST

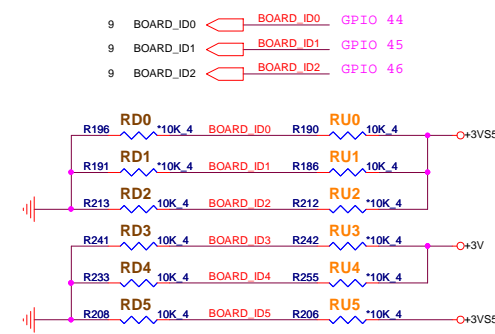


GPIO Pull-up/Pull-down(CLG)

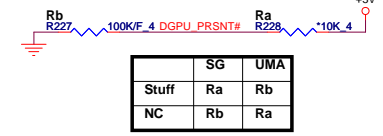


BOARD ID SETTING

BOARD ID SETTING	0	1
BOARD_ID0 GPIO 44	Micron	Hynix
BOARD_ID1 GPIO 45	non-beats	beats
BOARD_ID2 GPIO 46	on- board RAM	non-on board ram
BOARD_ID3 GPIO 34	RESERVE	RESERVE
BOARD_ID4 GPIO 35	RESERVE	RESERVE
BOARD_ID5 GPIO 24	RESERVE	RESERVE



GFX Present

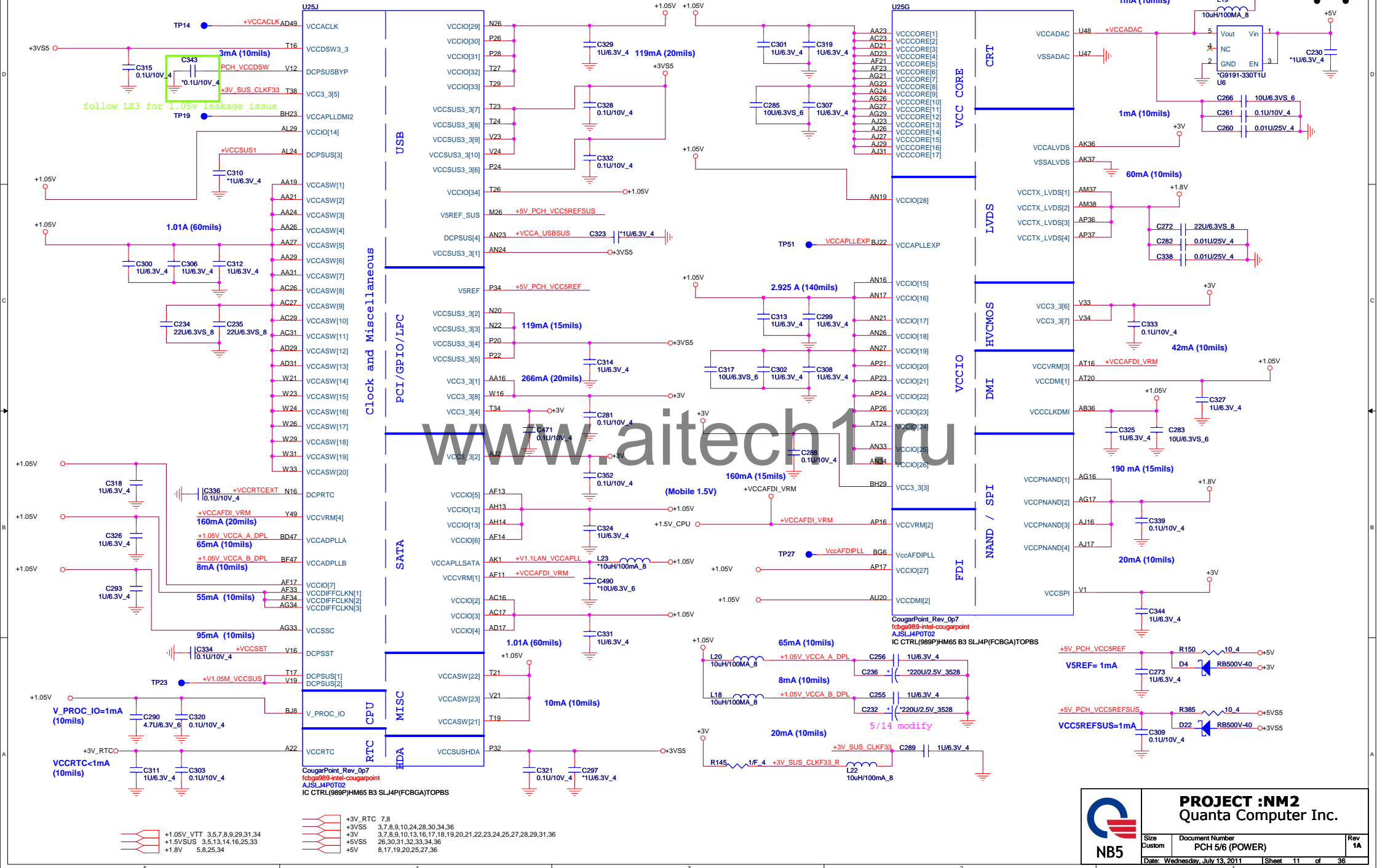


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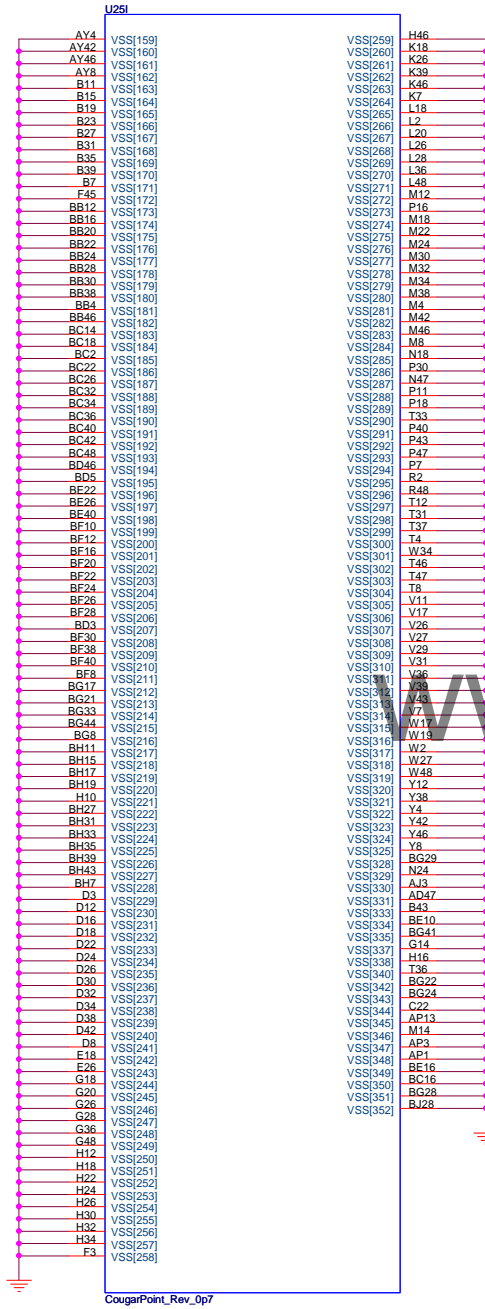
Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
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COUGAR POINT (POWER)

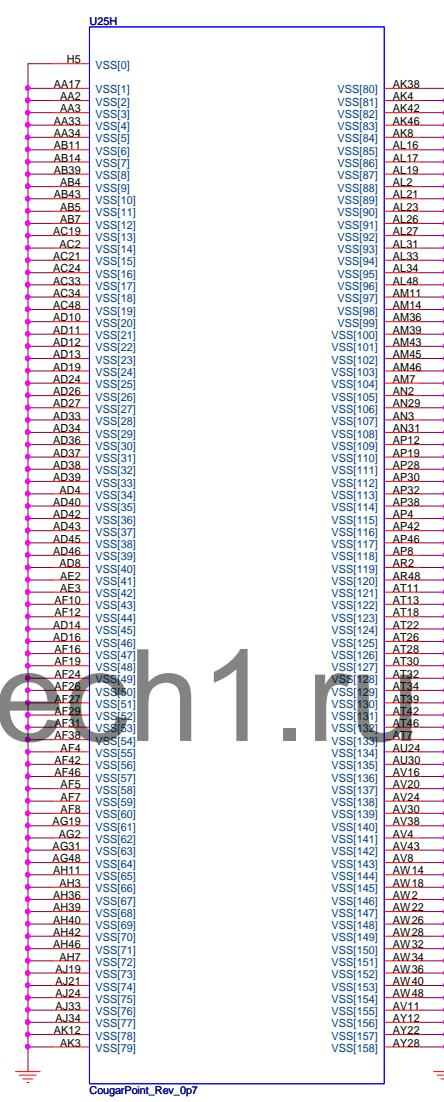
U25G

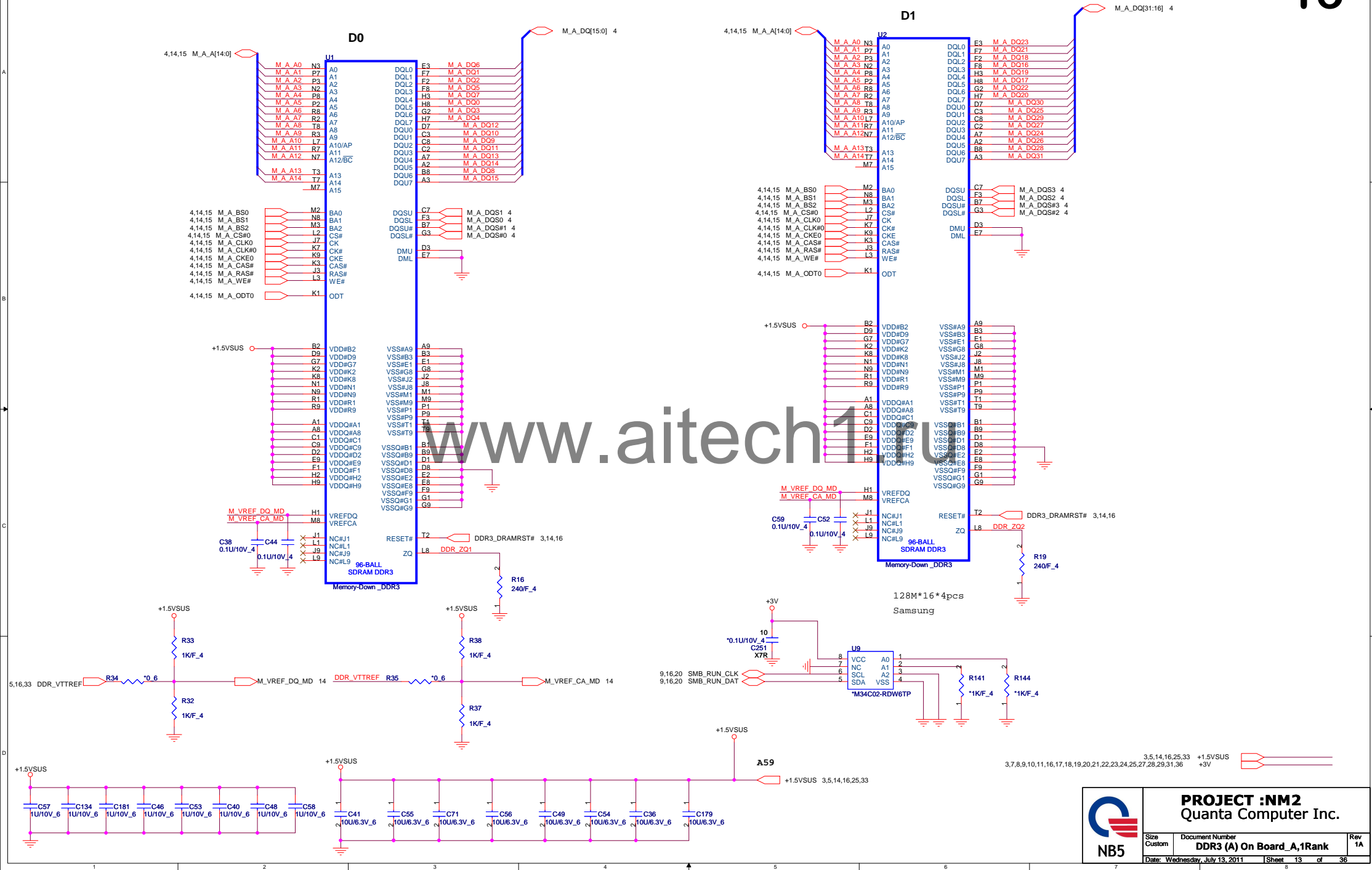


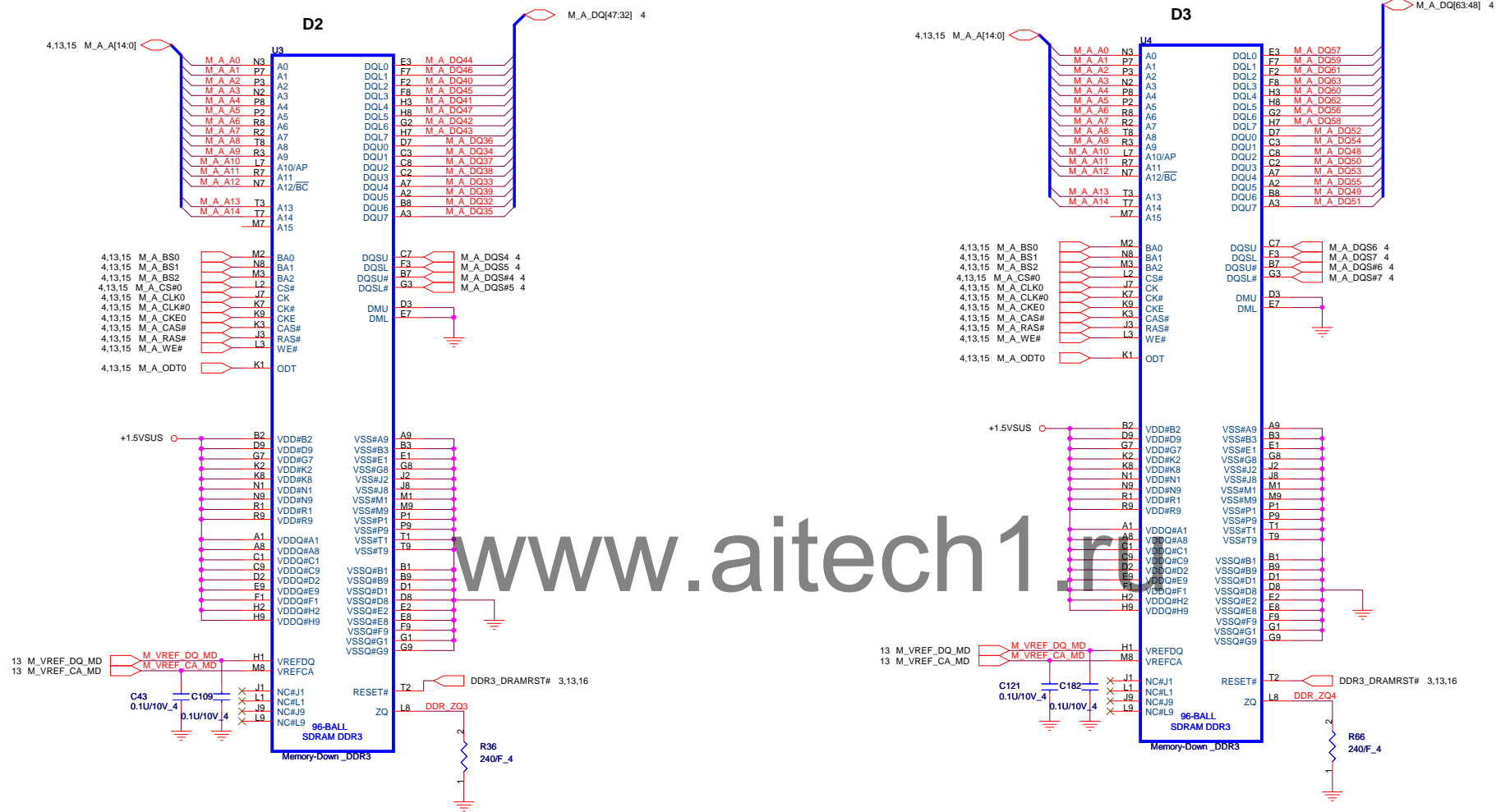
IBEX PEAK-M (GND)



IBEX PEAK-M (GND)

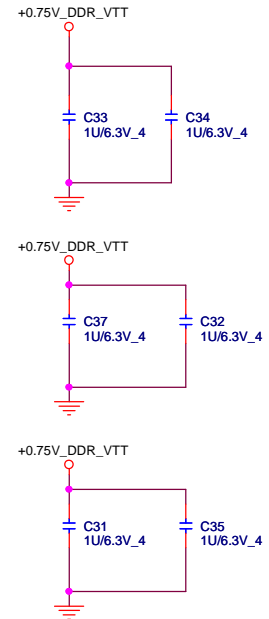
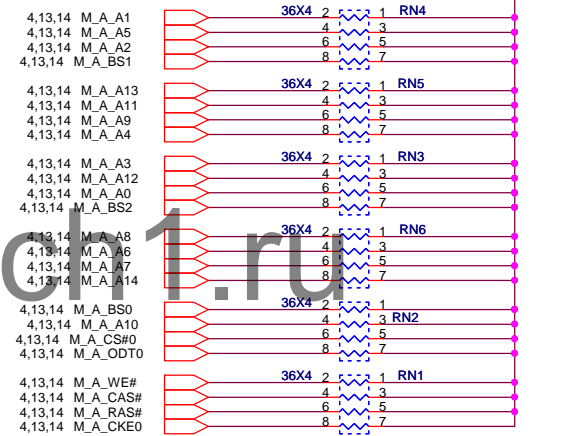






DDR3 TERMINATION FOR MEMORY DOWN

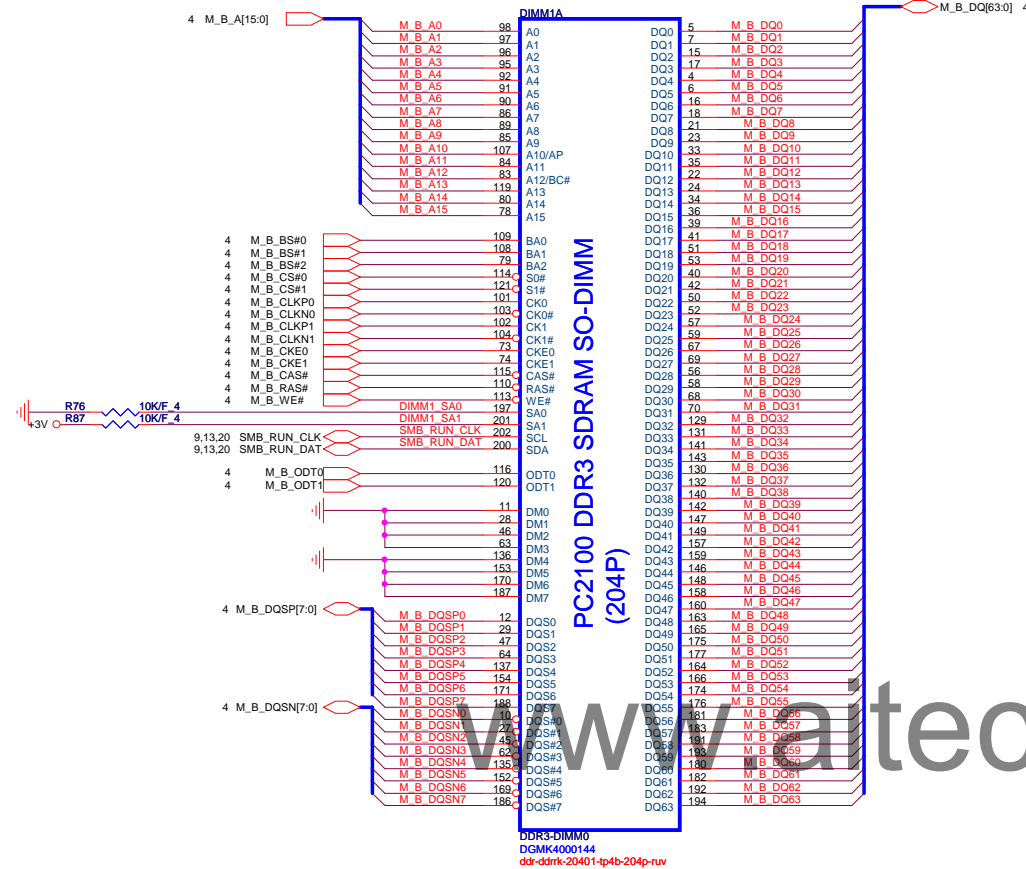
Please these resistor
closely DIMMA,all
trace length<750 mil.



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Size	Document Number	Rev
B	DDR3 TERMINATION	1A
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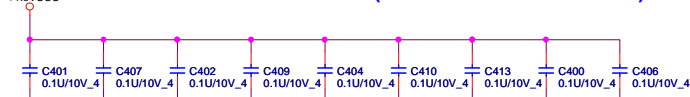
DDR_RVS (4.0mm)



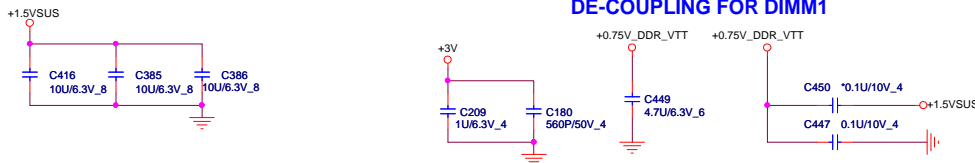
Place these Caps near So-Dimm1.

Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

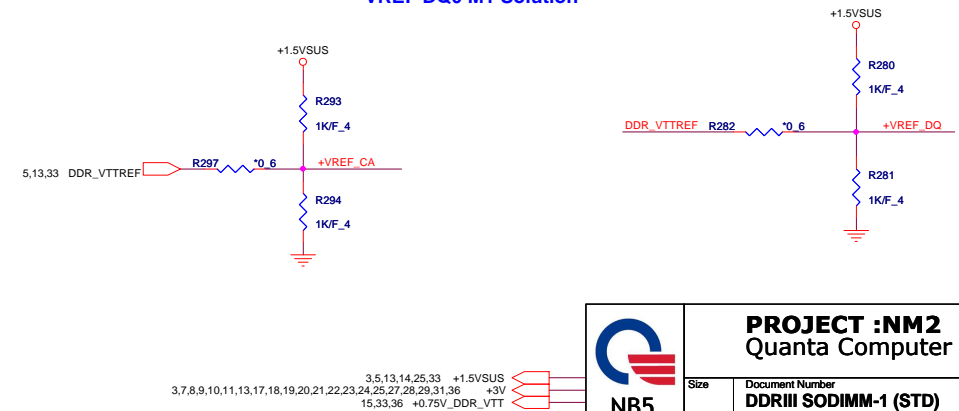
DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN)



DE-COUPLING FOR DIMM1



VREF DQ0 M1 Solution



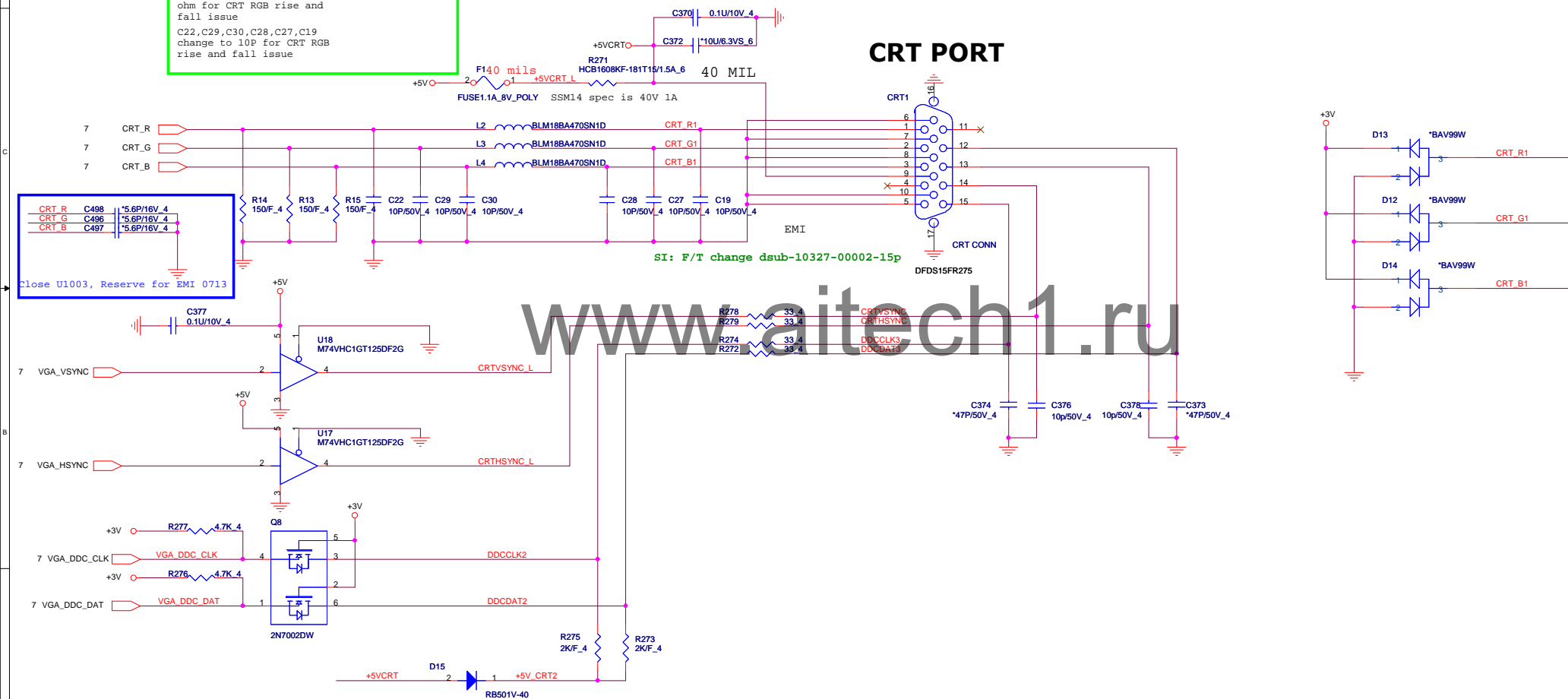
PROJECT :NM2
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	DDR3 SODIMM-1 (STD)	1A
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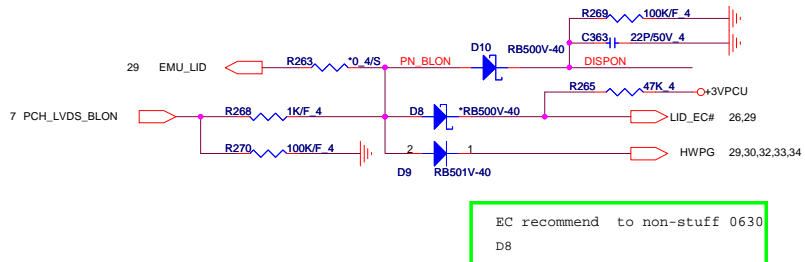
3,7,8,9,10,11,13,16,18,19,20,21,22,23,24,25,27,28,29,31,36 +3V
8,11,19,20,25,27,36 +5V

0707
L2,L3,L4 change to bead 47
ohm for CRT RGB rise and
fall issue
C22,C29,C30,C28,C27,C19
change to 10P for CRT RGB
rise and fall issue

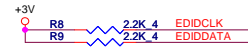
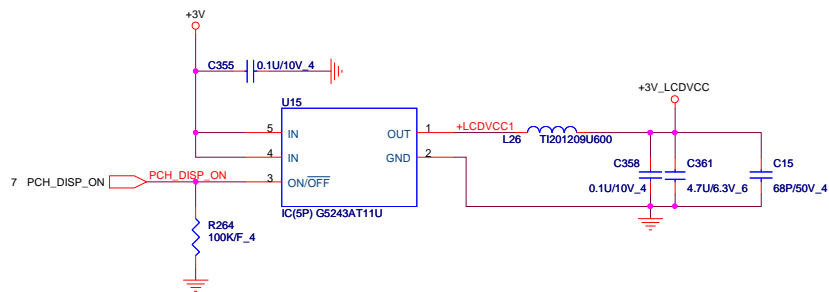
CRT PORT



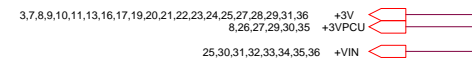
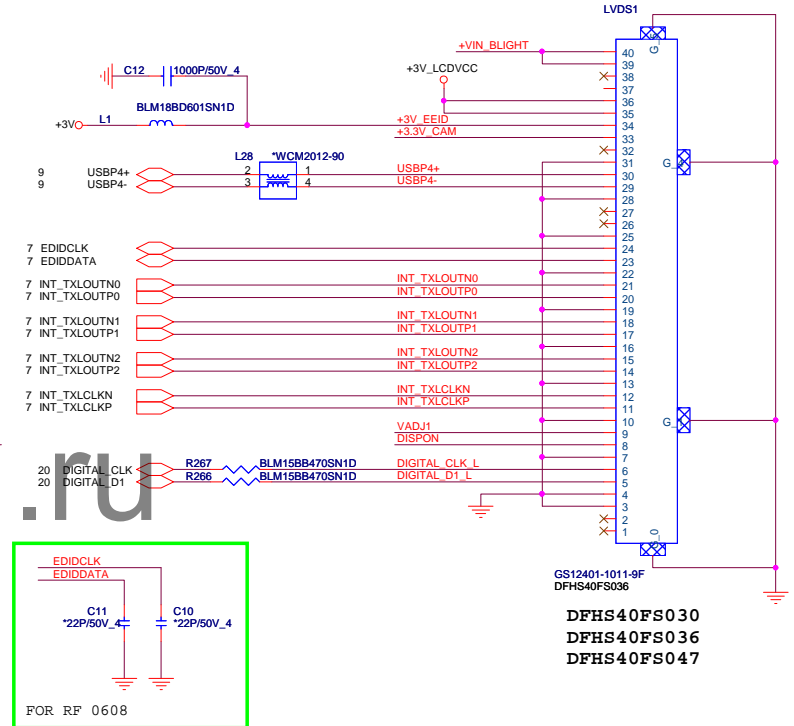
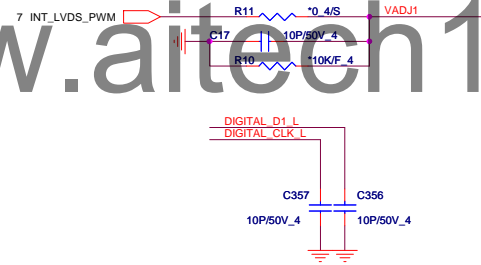
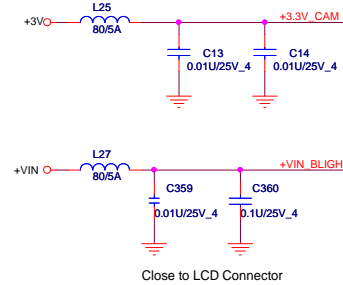
Backlight Control(LDS)

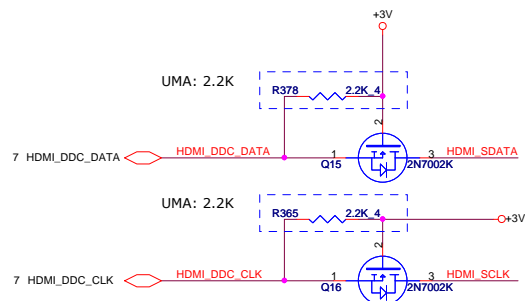
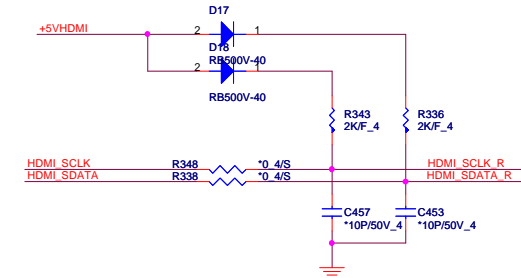
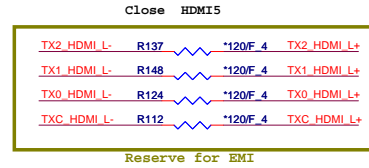
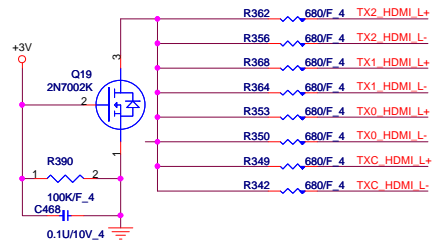


LCD POWER SWITCH

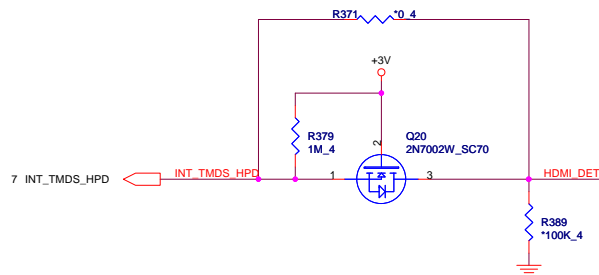


LED Panel(LDS)

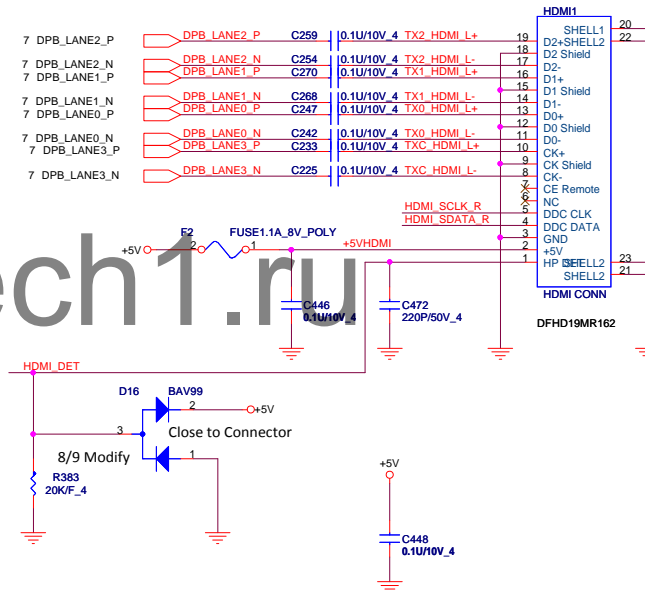




INT HDMI Detect Function



INT. HDMI



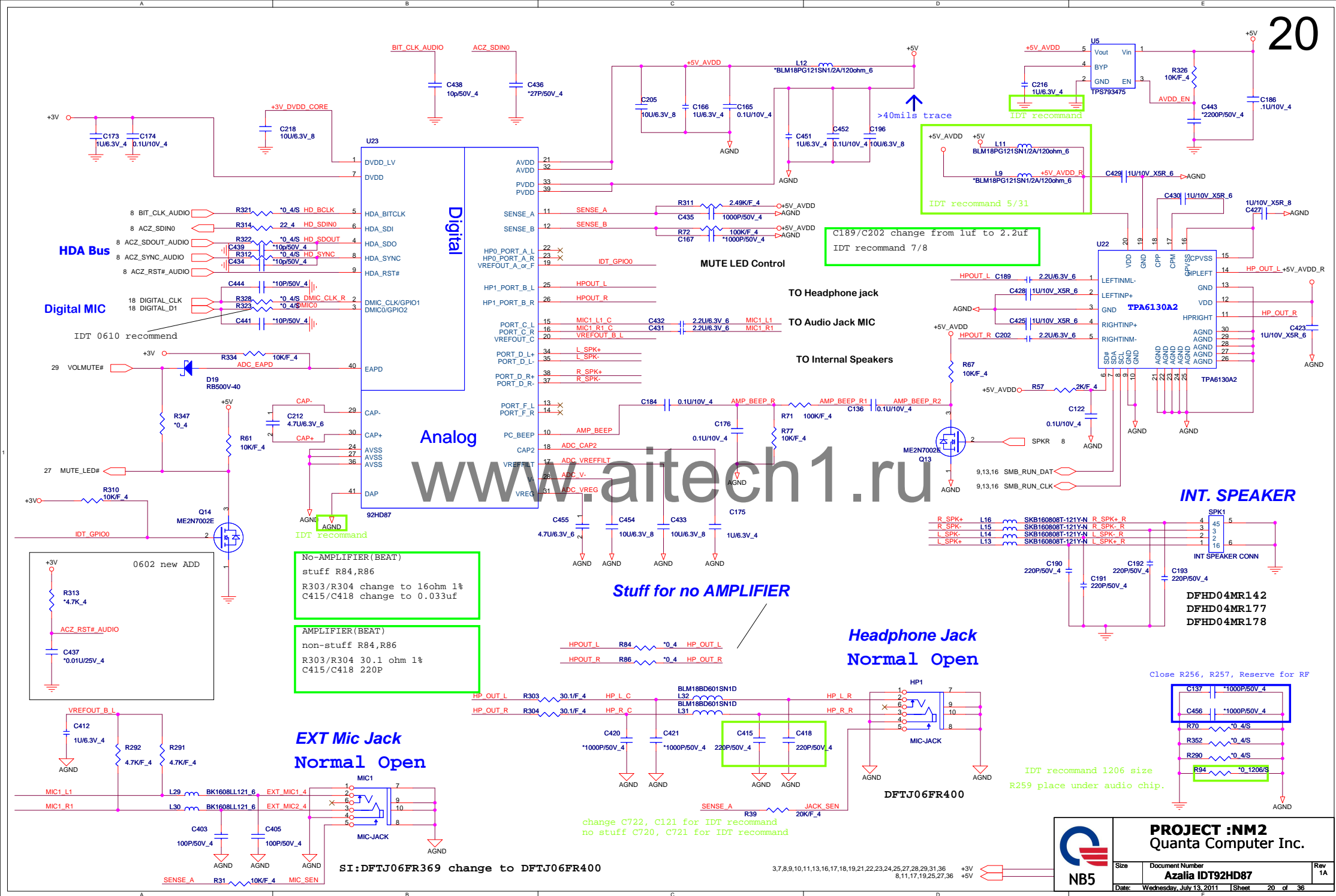
3,7,8,9,10,11,13,16,17,18,20,21,22,23,24,25,27,28,29,31,36
8,11,17,20,25,27,36

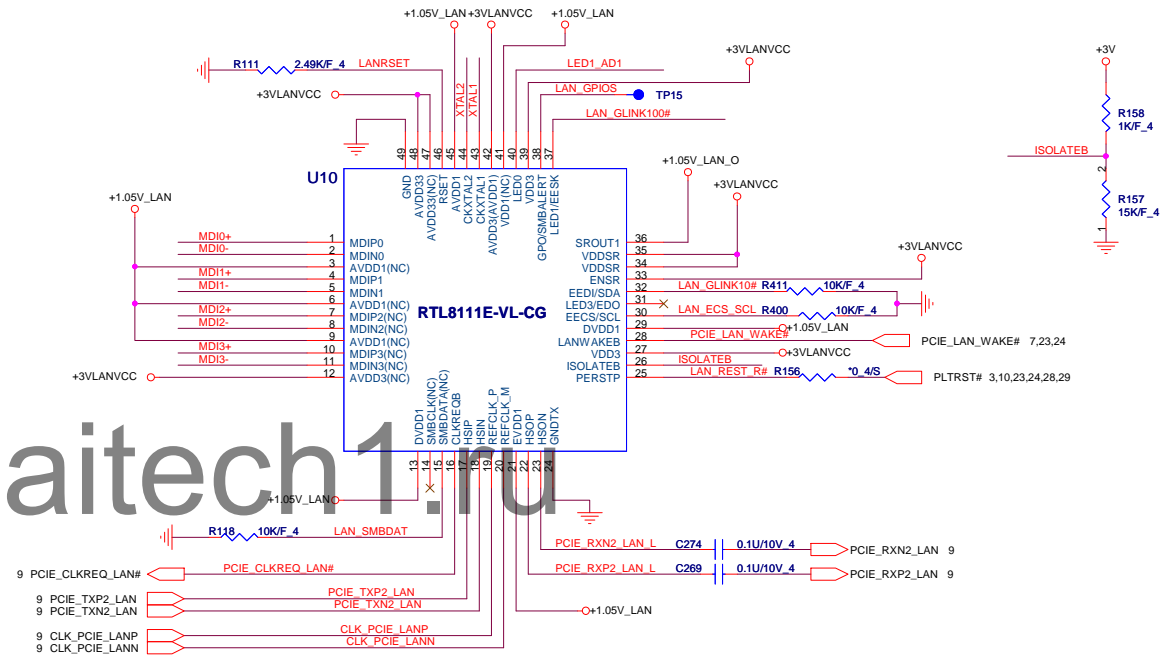
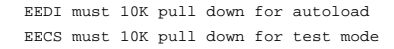
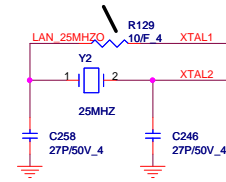
+3V
+5V



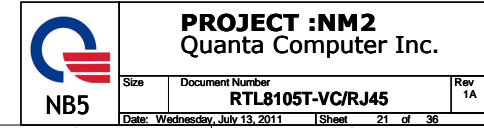
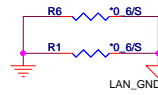
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HDMI Connector				
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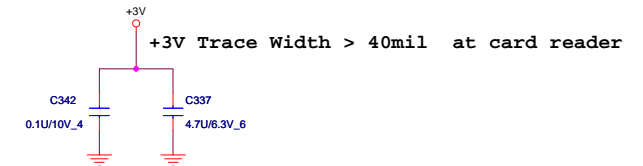
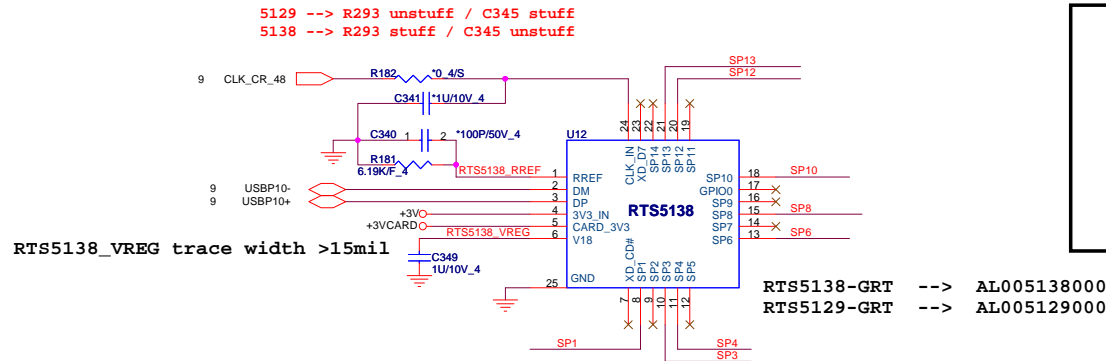


AL08111DB00 RTL8111DL-GR

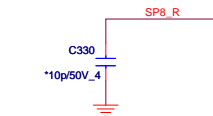
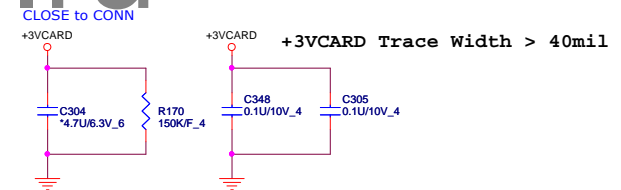
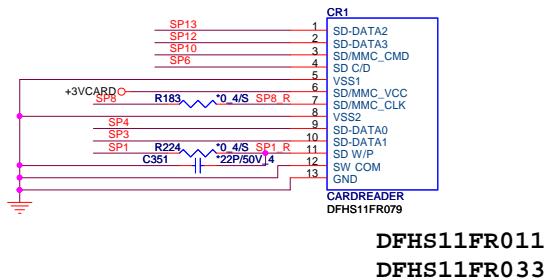


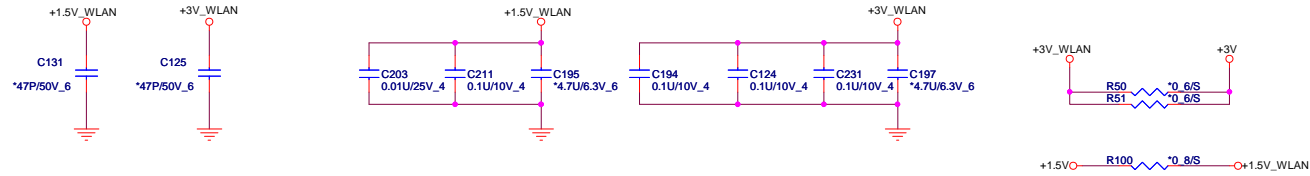
Share Pin

	XD_CD#	SD_WP	MS_CLK
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#	SD_D1	MS_INS#
SP3	XD_CE#	SD_D0	MS_D7
SP4	XD_CLE	SD_D7	MS_D3
SP5	XD_ALE	SD_D6	MS_D6
SP6	XD_WE#	SD_D5	MS_D0
SP7	XD_WP	SD_D4	MS_D4
SP8	XD_D0	SD_D3	MS_D1
SP9	XD_D1	SD_D2	MS_D5
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6	SD_D1	MS_BS
	XD_D7		



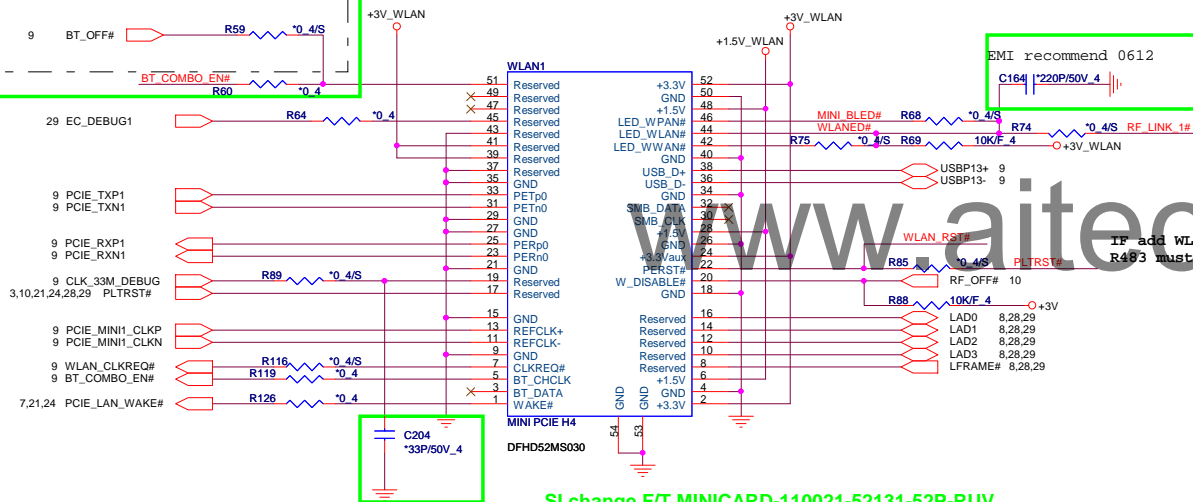
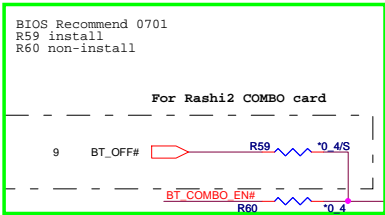
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SD / MMC
CARD READER



Mini PCI-E Card 1 Half Mini PCI-E WLAN

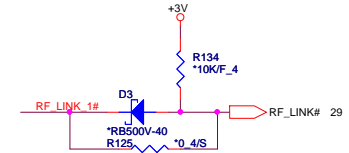
The value of the capacitor is suggest by Siemens HQ expert.
For against 900MHz RF interference. The value of capacitor is 27pF.
For against 1800MHz RF interference. The value of capacitor is 10pF.
1nF/10nF value capacitor use for against ESD purpose.



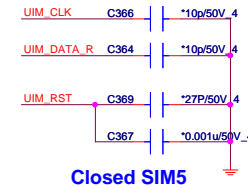
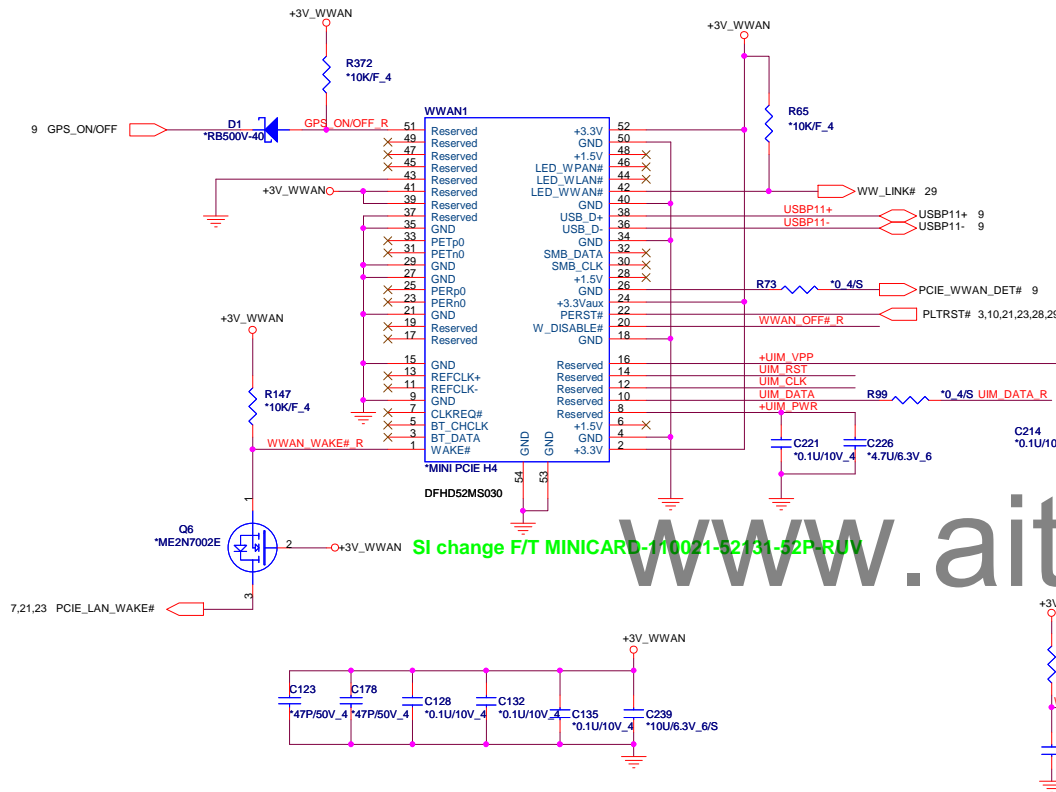
SI:RF solution

SI change F/T MINICARD-110021-52131-52P-RUV

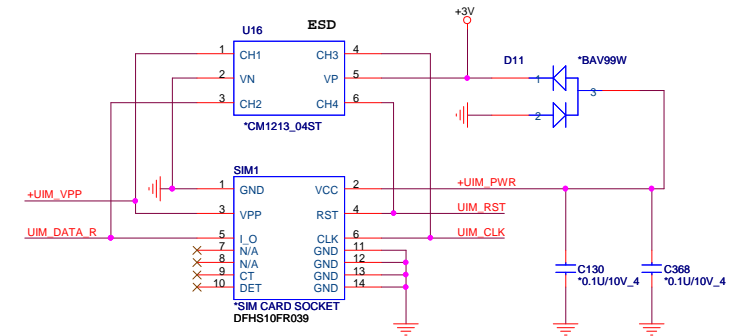
IF add WLAN_RST# schematic
R483 must change to 10K



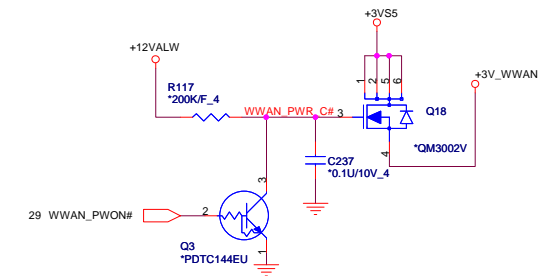
Full mini PCIE for WWAN Mini PCI-E Card 2



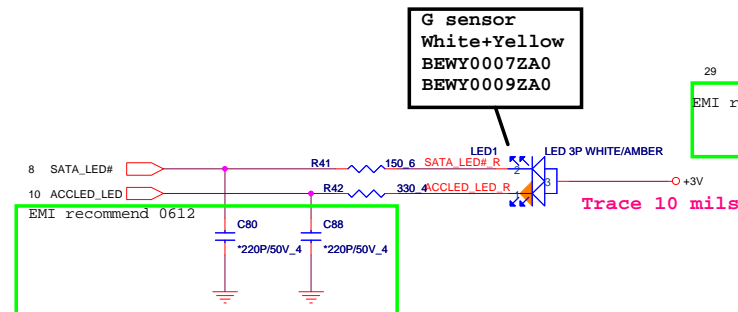
SIM CARD SIGNALS ROUTE PARALLEL



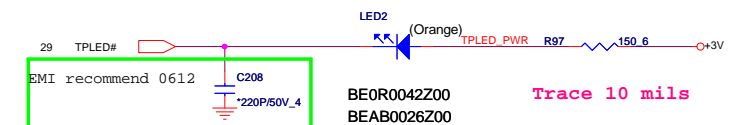
SIM CARD



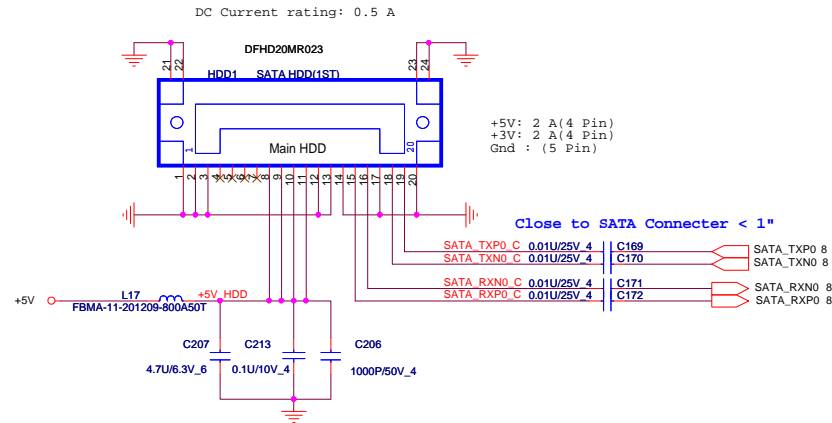
SATA/G sensor LED



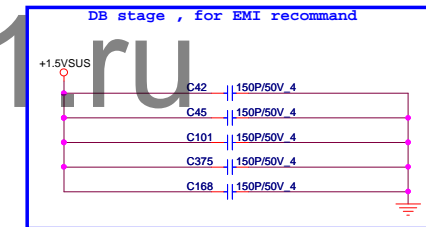
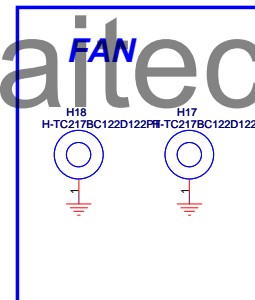
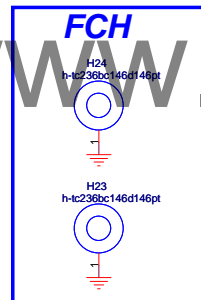
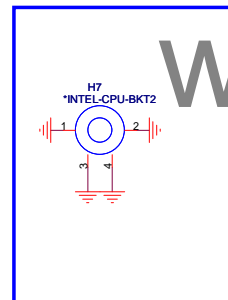
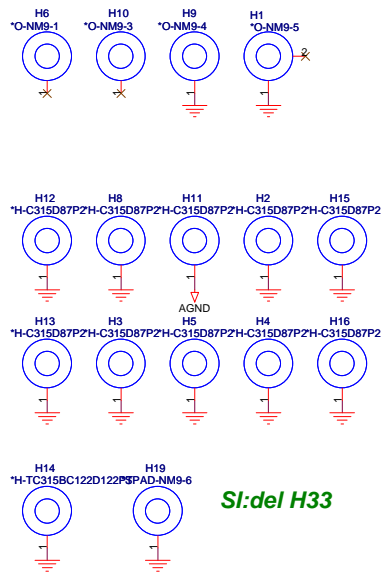
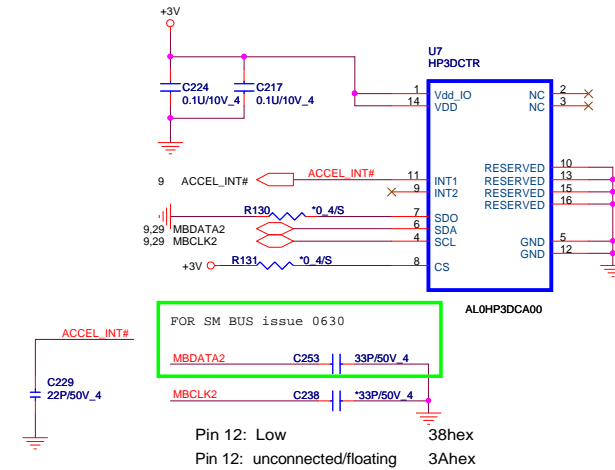
Touchpad LED



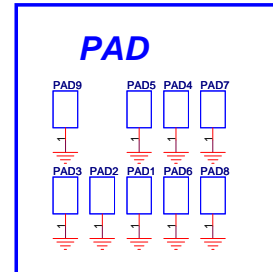
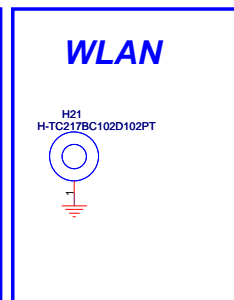
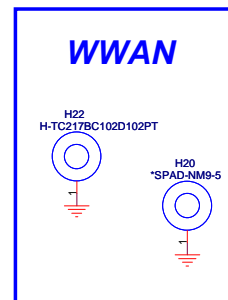
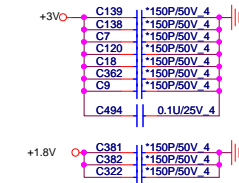
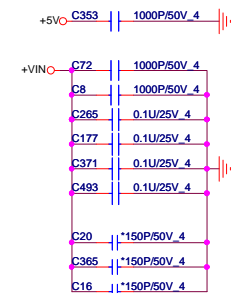
2.5" SATA HDD OR SSD(TOSHIBA)



Accelerometer Sensor



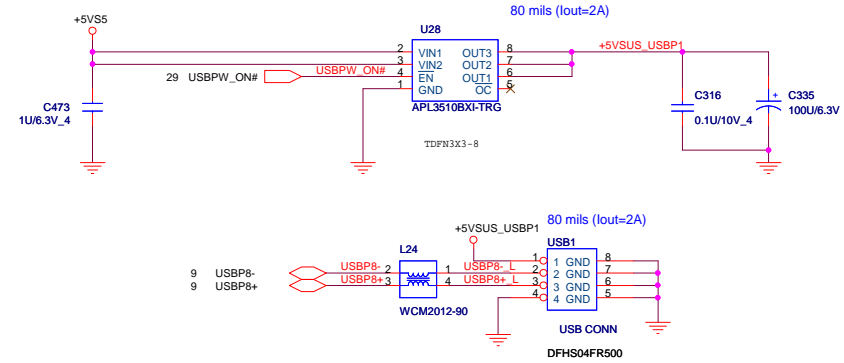
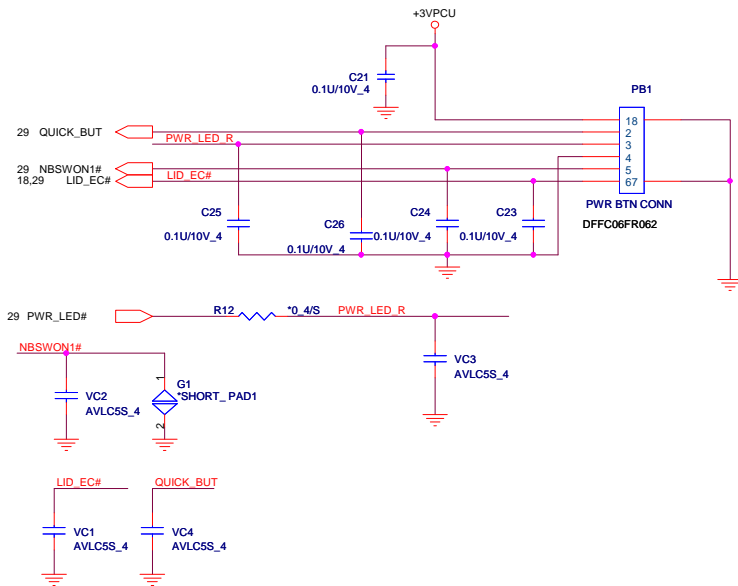
PRE- PV stage , for RF recommand



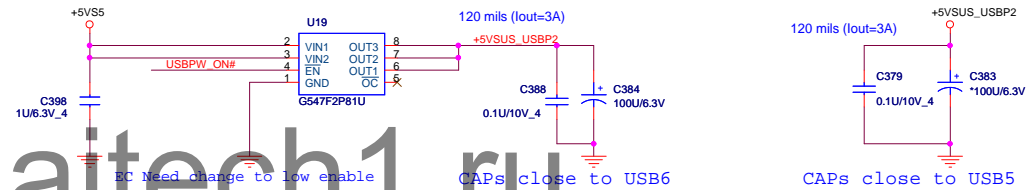
PROJECT :NM2
Quanta Computer Inc.

Size	Document Number HDD/Hole/G Senser/RF	Rev 1A
Date: Wednesday, July 13, 2011	Sheet 25 of 36	

1x Left side USB port supports Keyed USB.



For Right 2xUSB Ports PWR

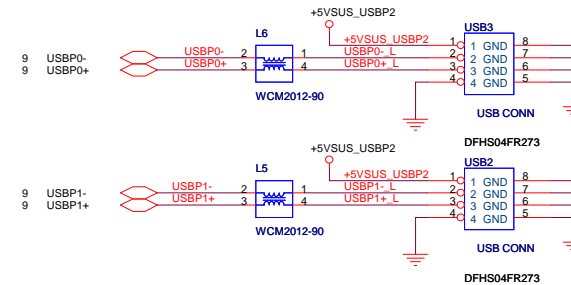


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EC Need change to low enable

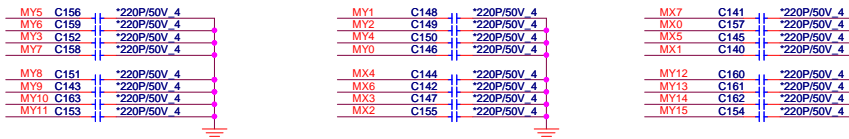
CAPs close to USB6

CAPs close to USB5

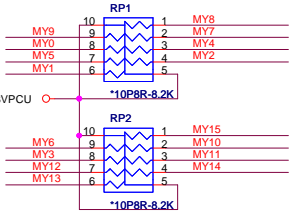


+3VPCU 8,18,27,29,30,35
+3V 3,7,8,9,10,11,13,16,17,18,19,20,21,22,23,24,25,27,28,29,31,36

Keyboard (KBC)



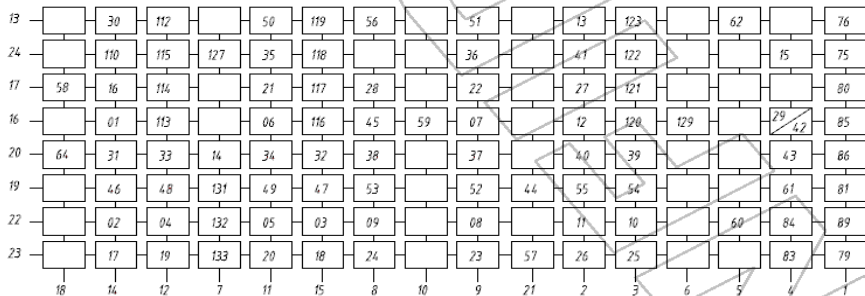
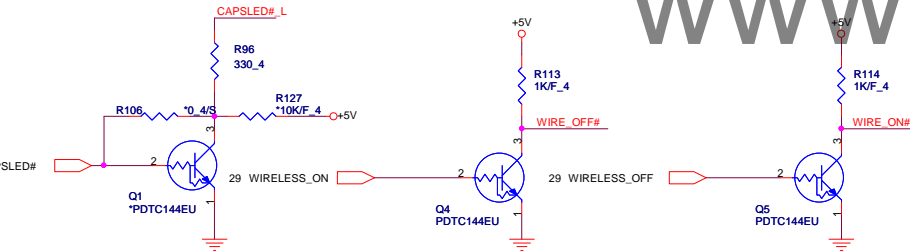
KEYBOARD PULL-UP



MY[0..15] MY[0..15]
MX[0..7] MX[0..7]

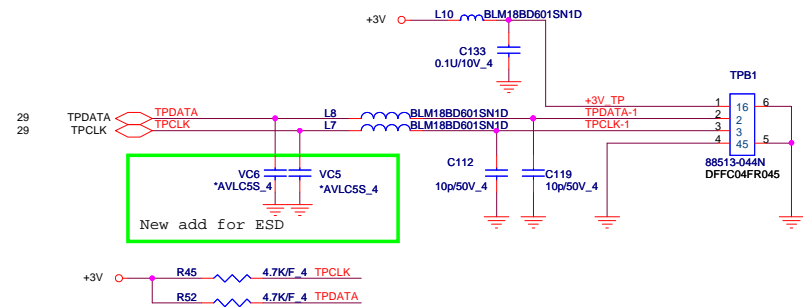
Enable WLAN --> wire_on high and wire_off low
Disable WLAN --> wire_on low and wire_off high

CAPSLED# high --> LED non-light
CAPSLED# low --> LED light

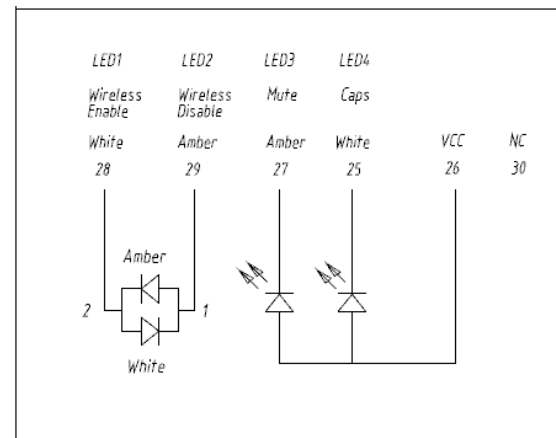
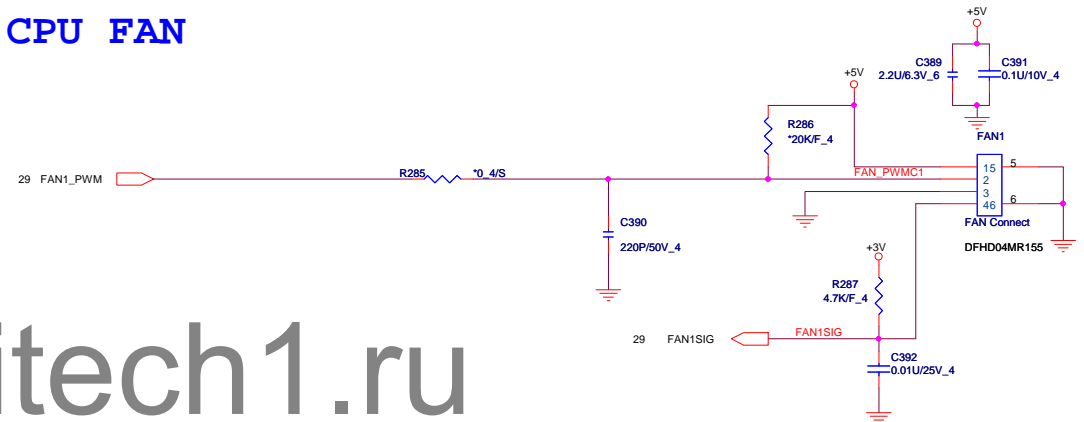


US MATRIX

TOUCH PAD CONN



CPU FAN




Pin 32

Pin 1

27

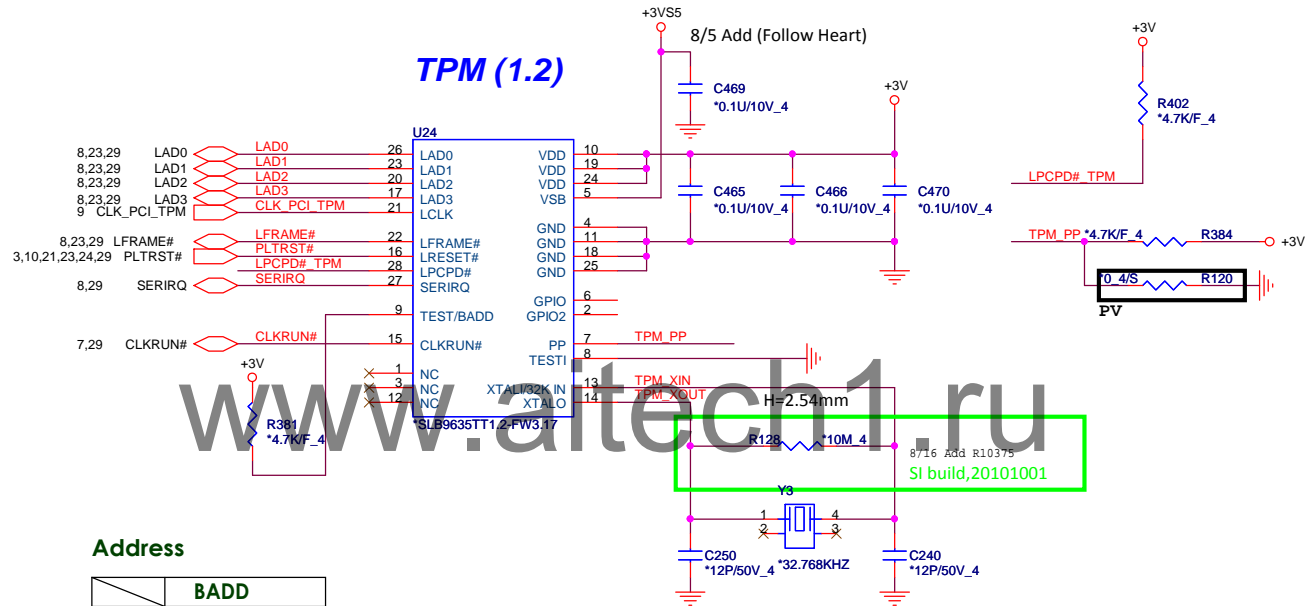
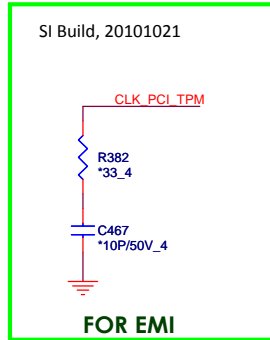
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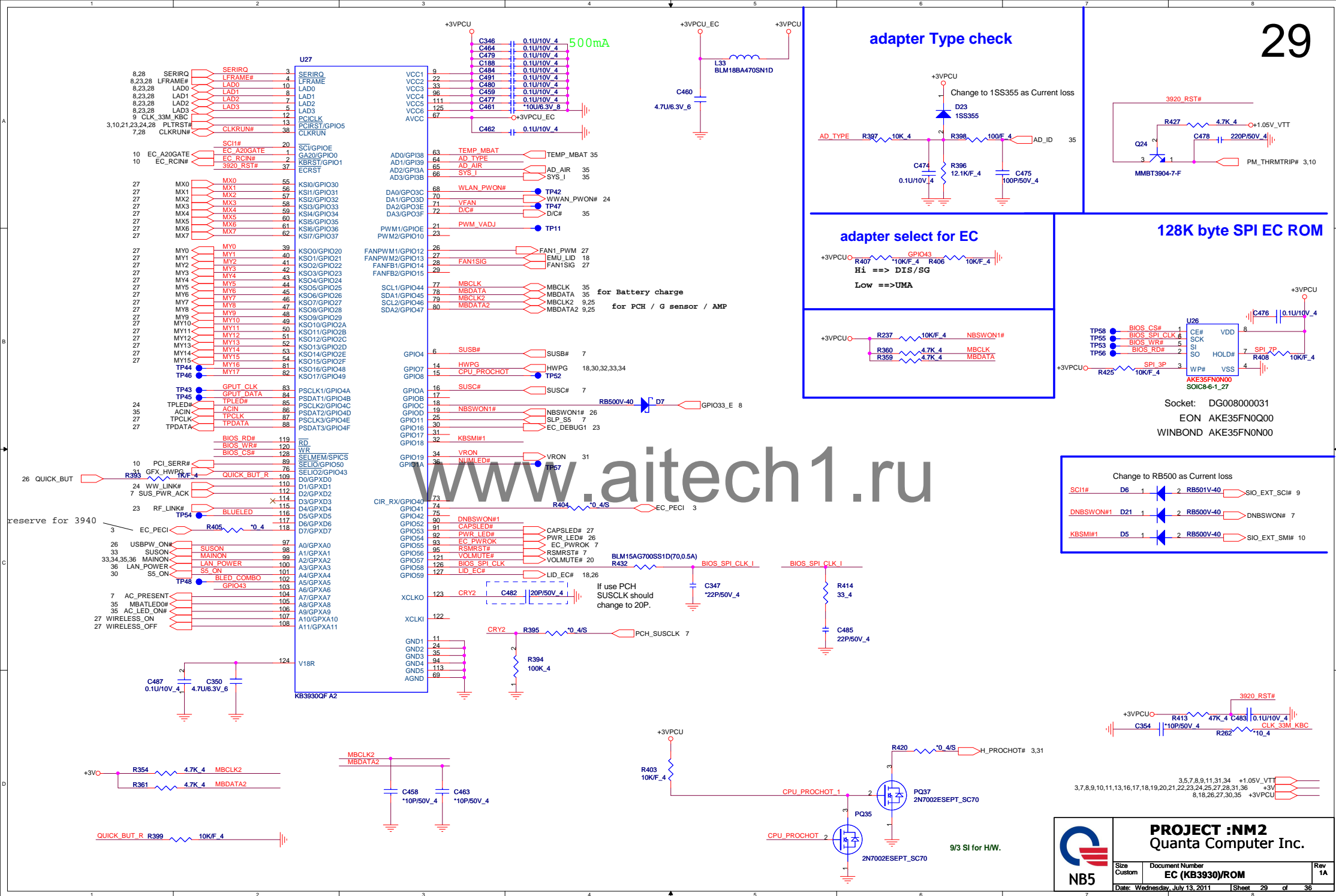
			PROJECT :NM2 Quanta Computer Inc.		
Size	Document Number	KB/TP/CPU FAN			Rev 1A
Date:	Wednesday, July 13, 2011 Sheet 27 of 36				

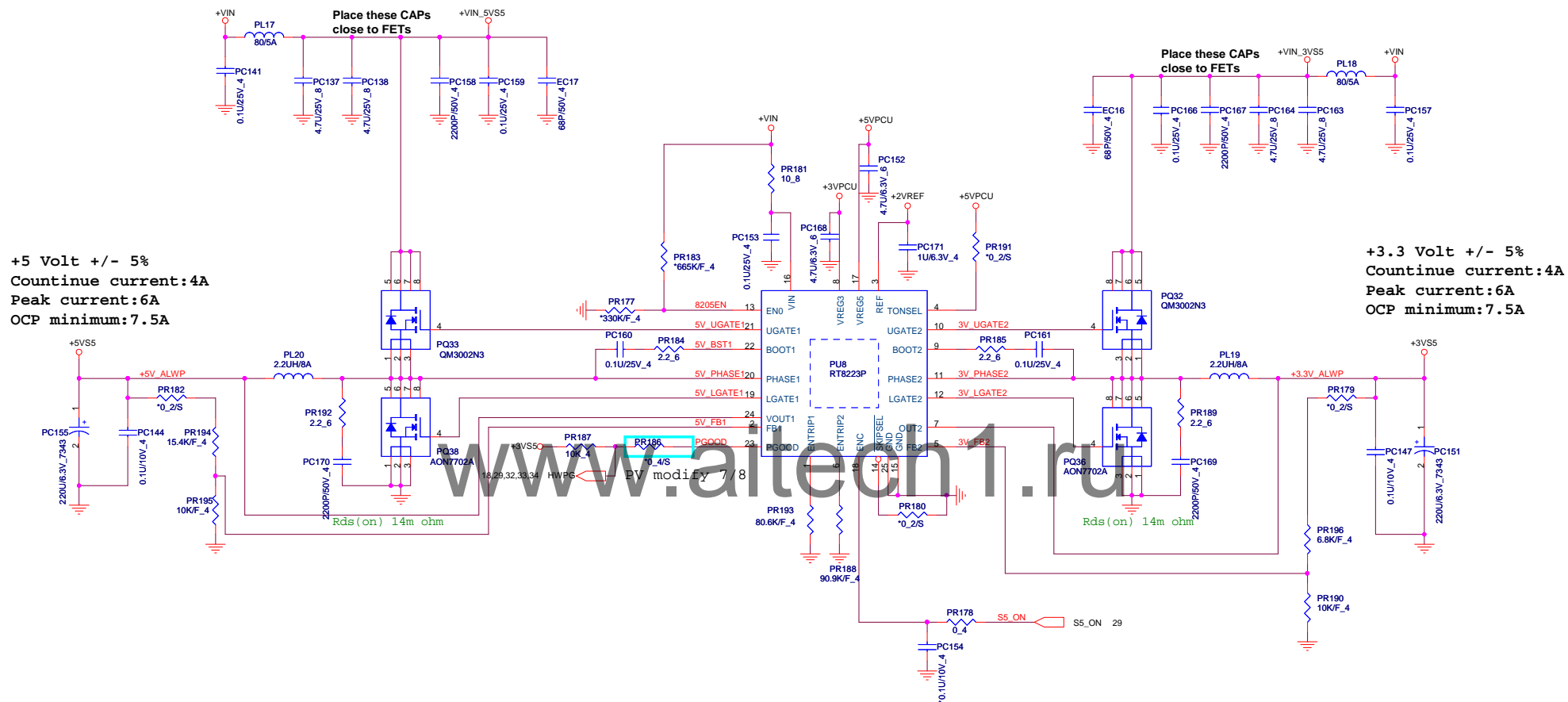
Charge LED

3 pins

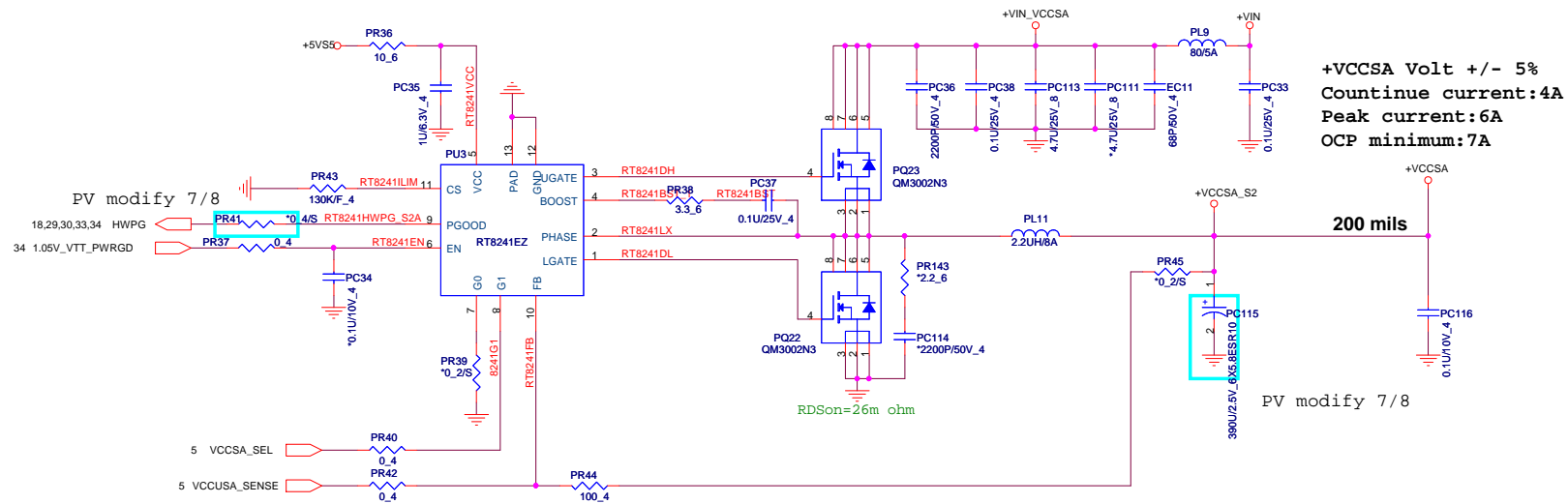
8,18,26,29,30,35 +3VPCU
8,11,17,19,20,25,36 +5V
3,7,8,9,10,11,13,16,17,18,19,20,21,22,23,24,25,28,29,31,36 +3V









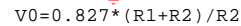
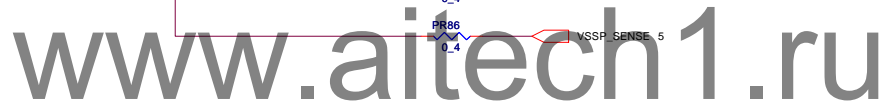


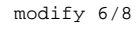
CPU system agent
voltage slew rate of 0.5 -10 mV/ μ s

H_FC_C22	VCCSA_SEL	Vout
VID0	VID1	
0	0	0.9V
0	1	0.80V (SV-RT8241DZGQW) 0.85V (LV-RT8241EZGQW)
1	0	0.725V
1	1	0.675V



2





Do Not add test pad on BATDIS_G signal

Place this ZVS close to
Diode away +VIN

Place this ZVS close to
Far-Far away of +VIN

**Place this cap
close to EC**

Place this cap

Place this cap
close to EC

PV modify 7/13

